FIG. 1

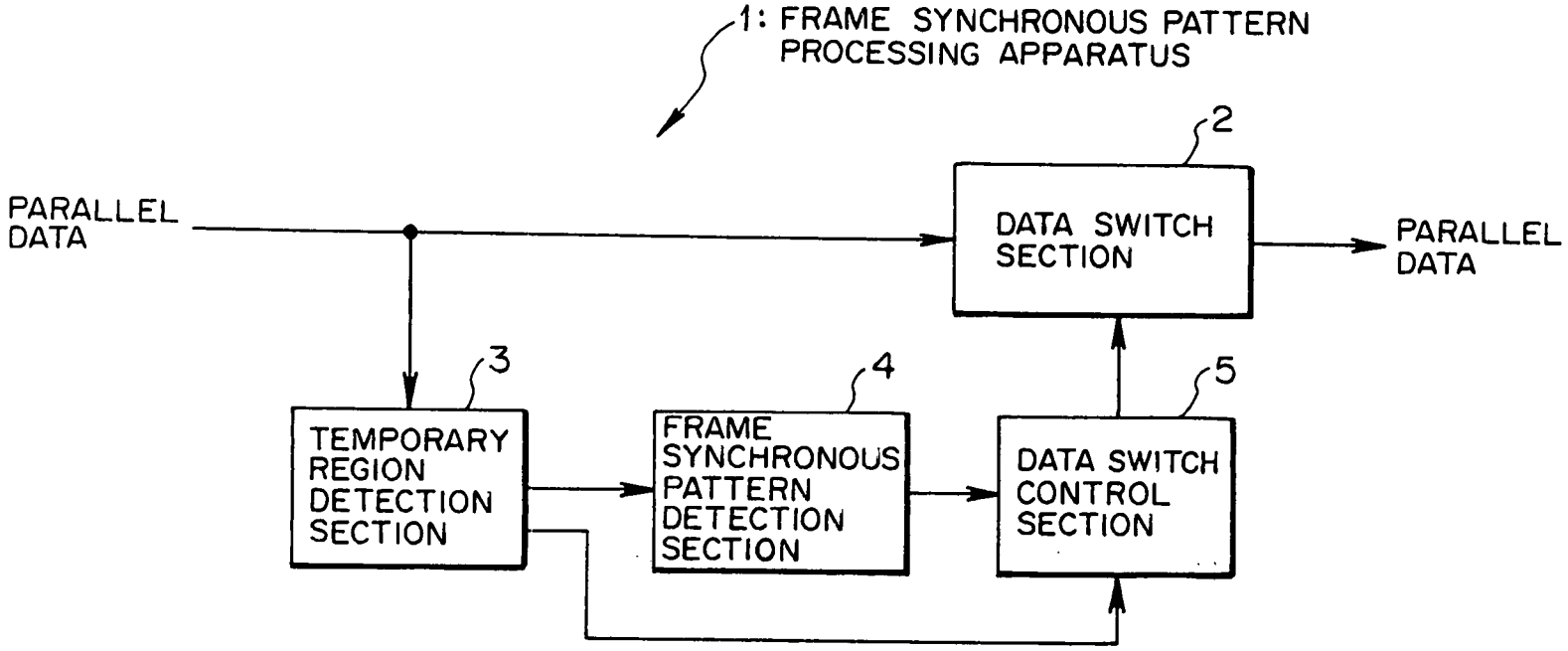


FIG. 2

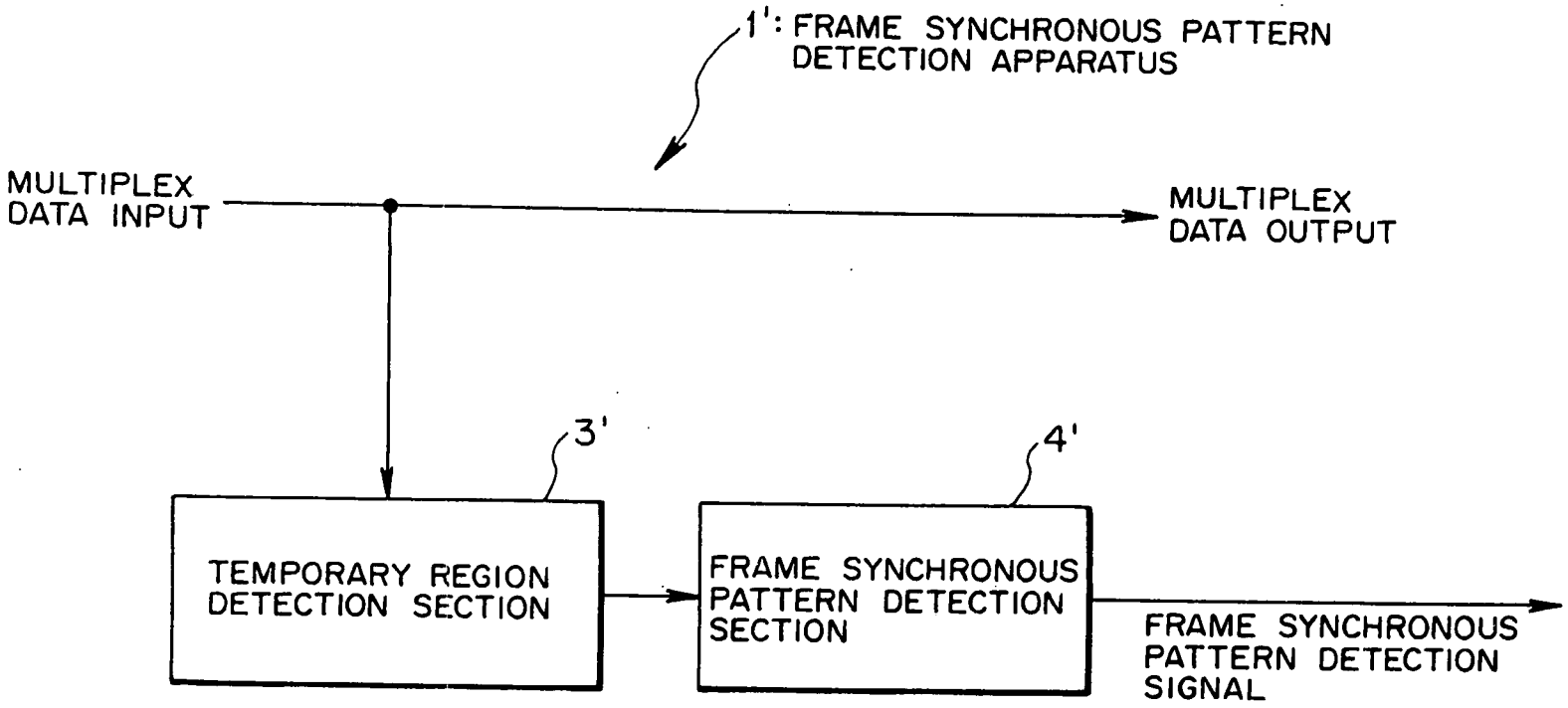


FIG.3

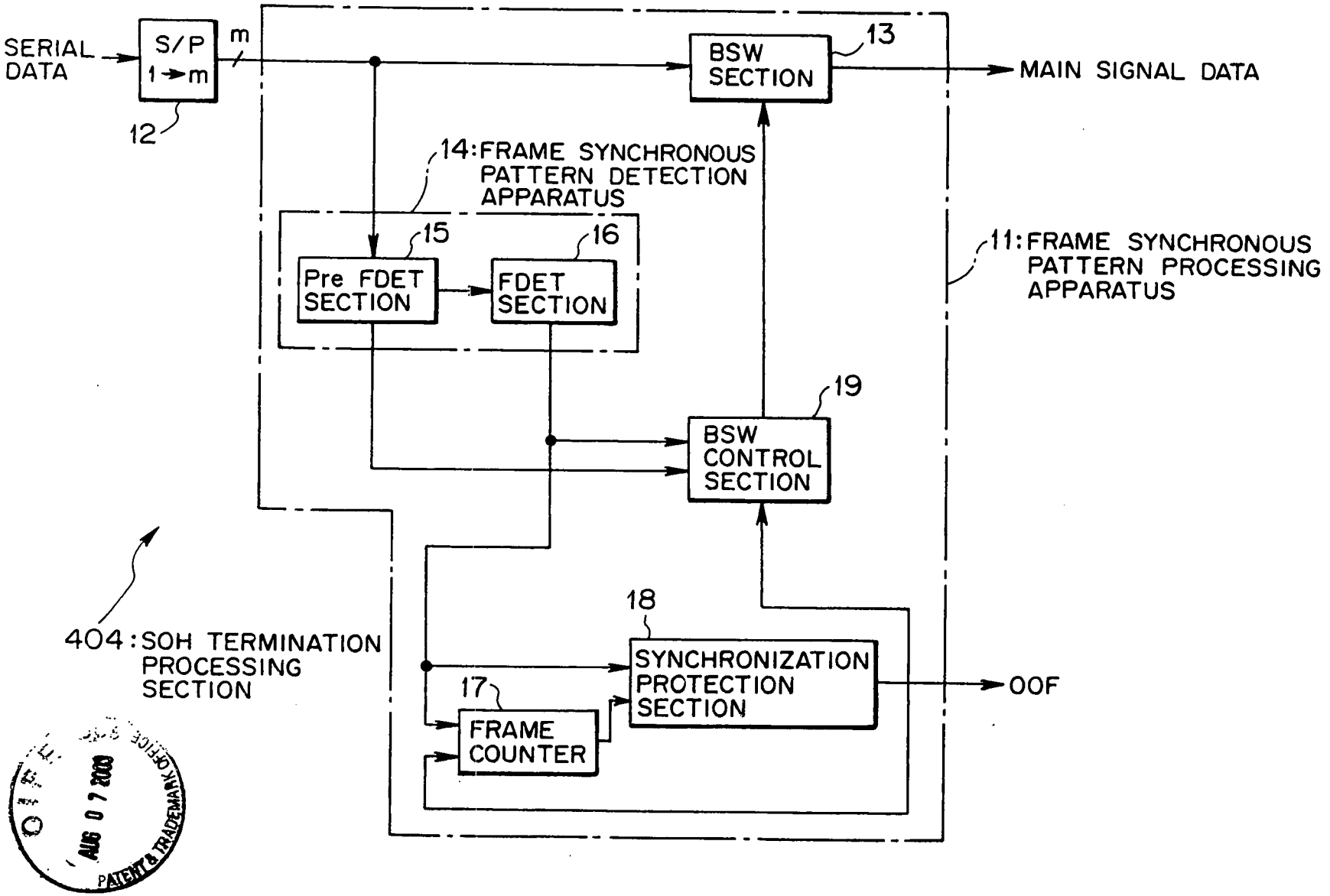


FIG. 4

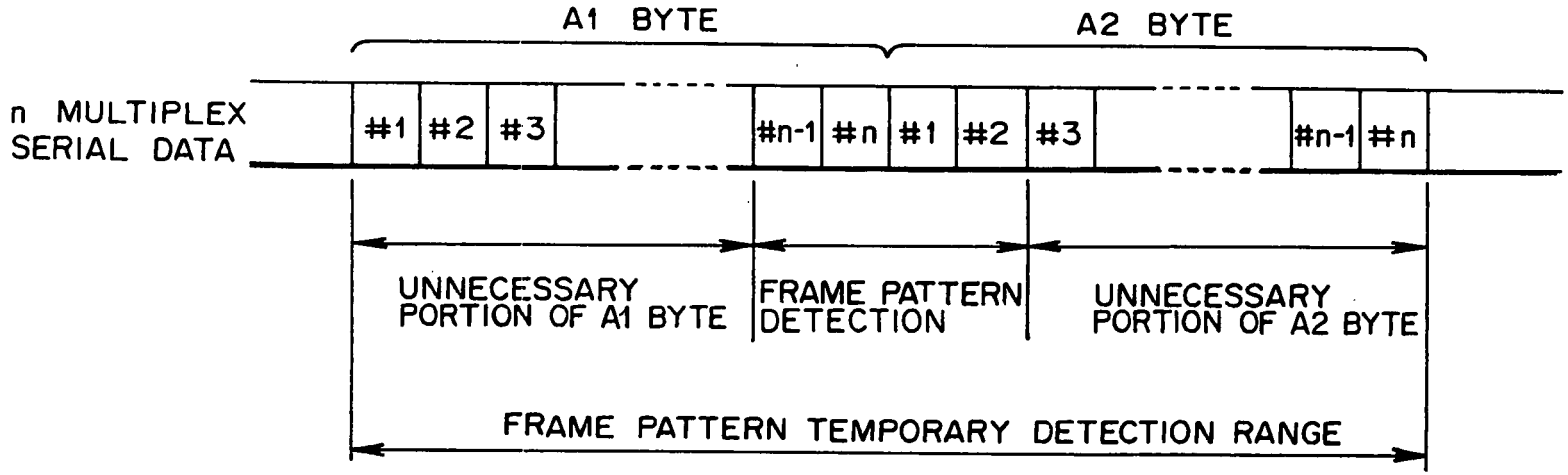


FIG.5

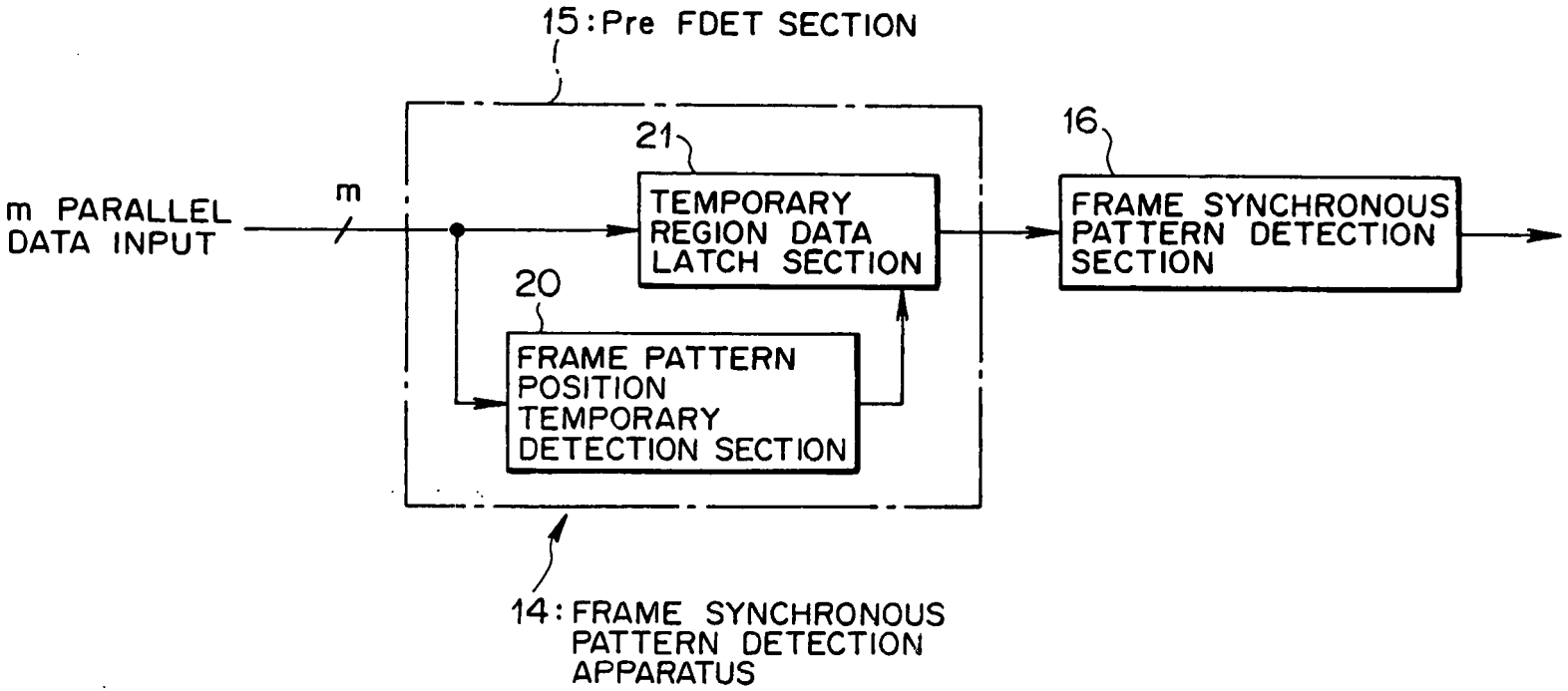


FIG.6

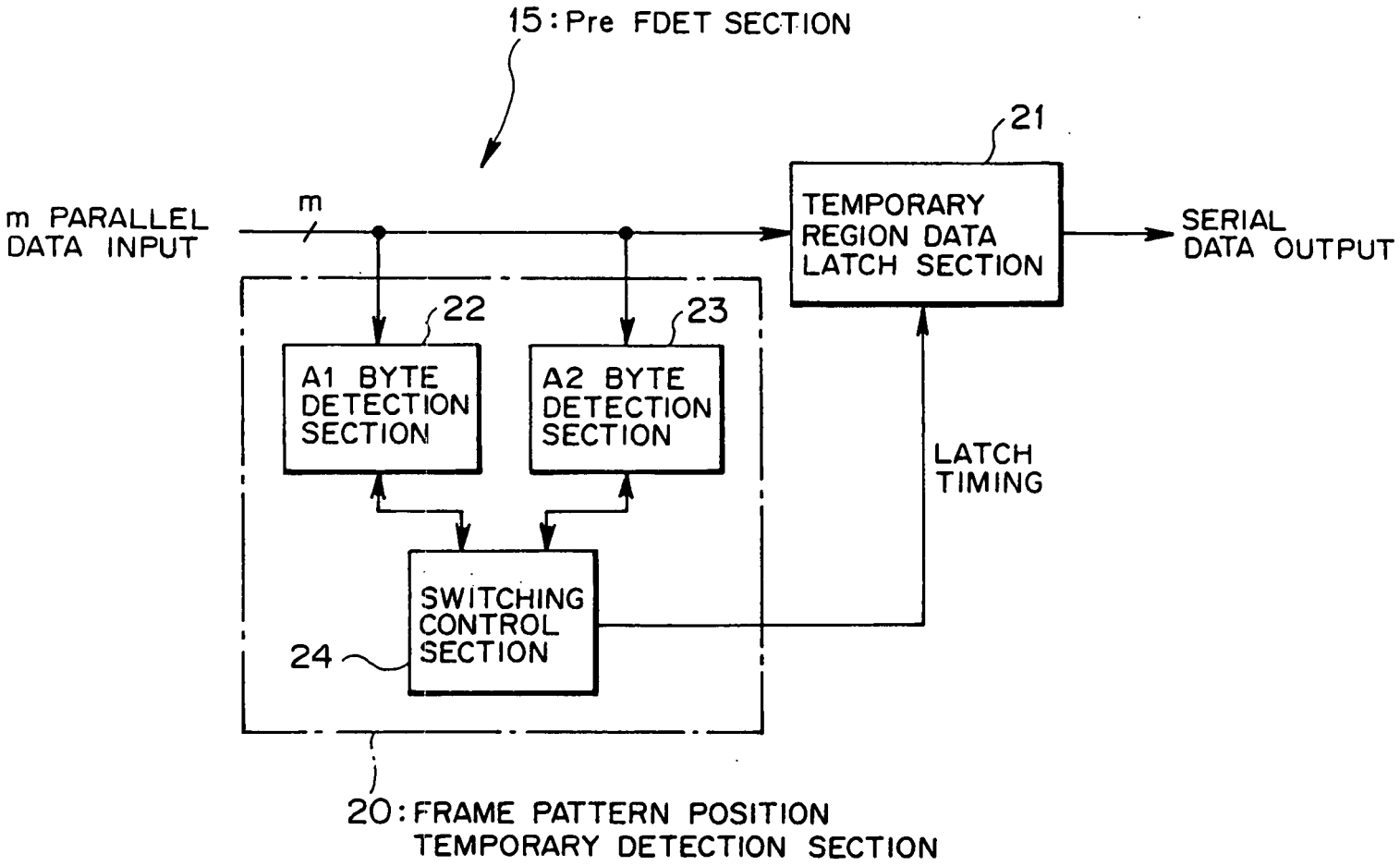

15 : Pre FDET SECTION
21
m PARALLEL DATA INPUT
m
TEMPORARY REGION DATA LATCH SECTION
SERIAL DATA OUTPUT
22
23
A1 BYTE DETECTION SECTION
A2 BYTE DETECTION SECTION
LATCH TIMING
SWITCHING CONTROL SECTION
24
20 : FRAME PATTERN POSITION TEMPORARY DETECTION SECTION

FIG. 7

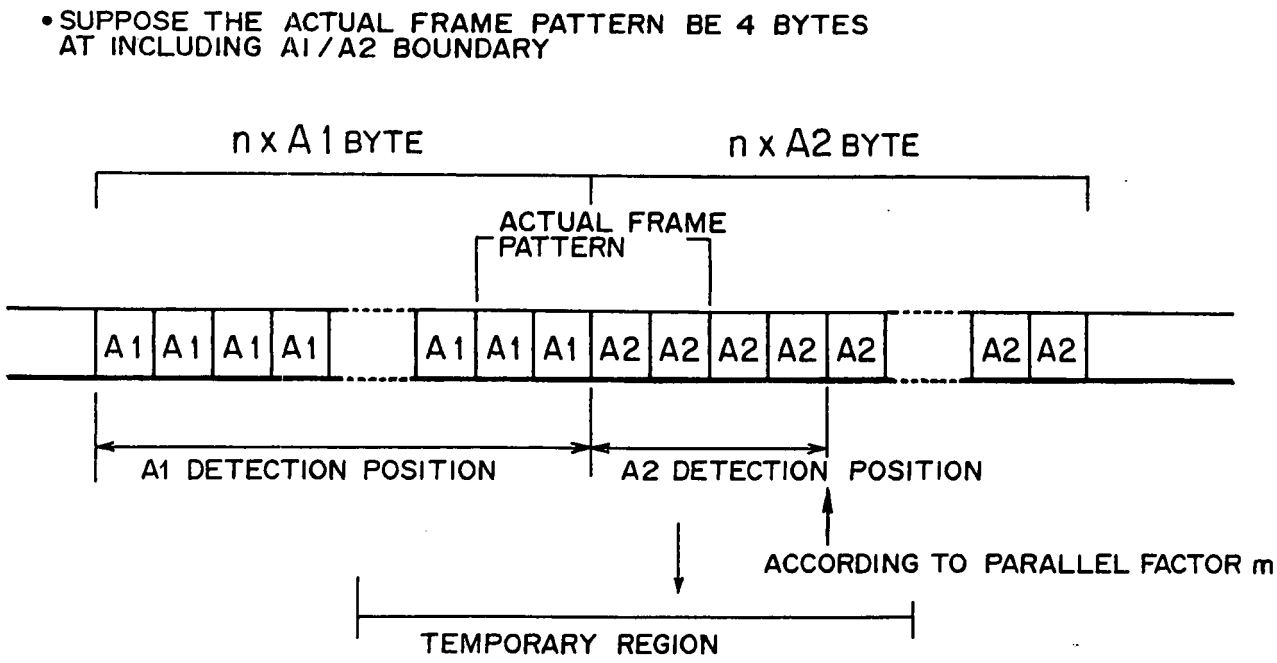


FIG. 8

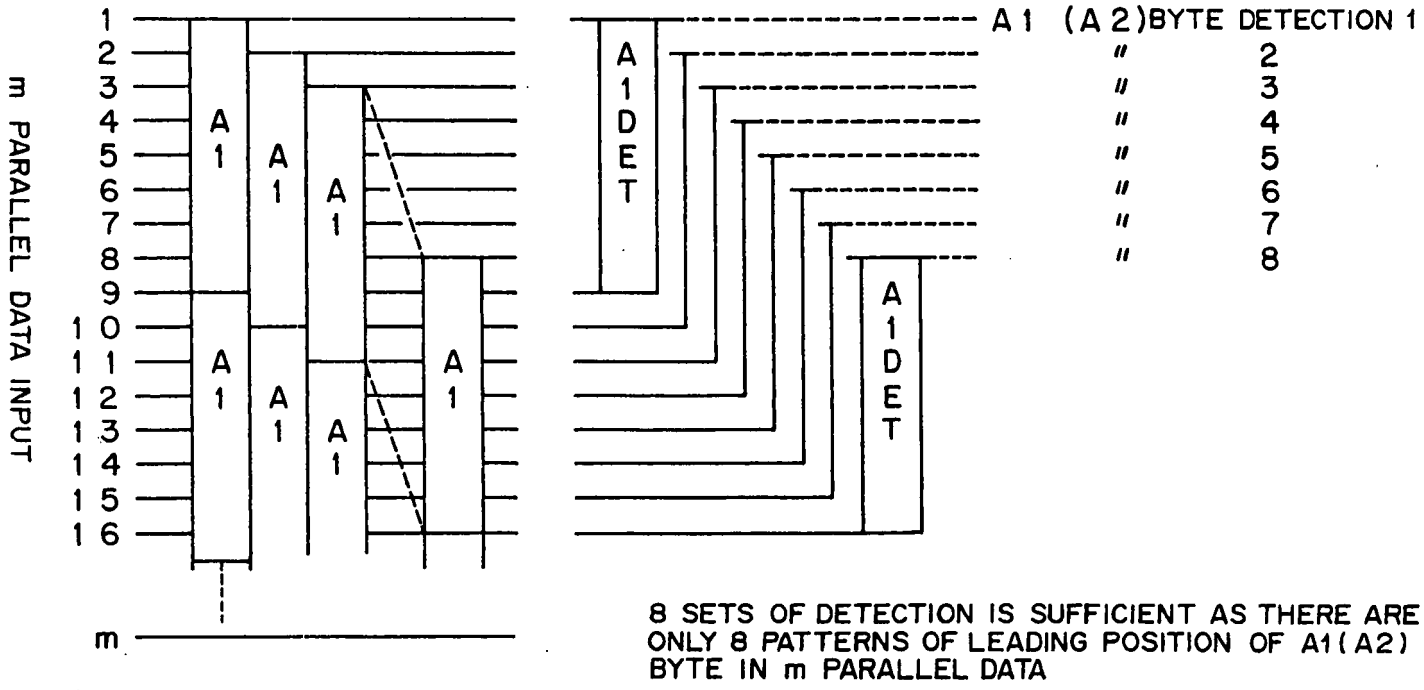


FIG. 9

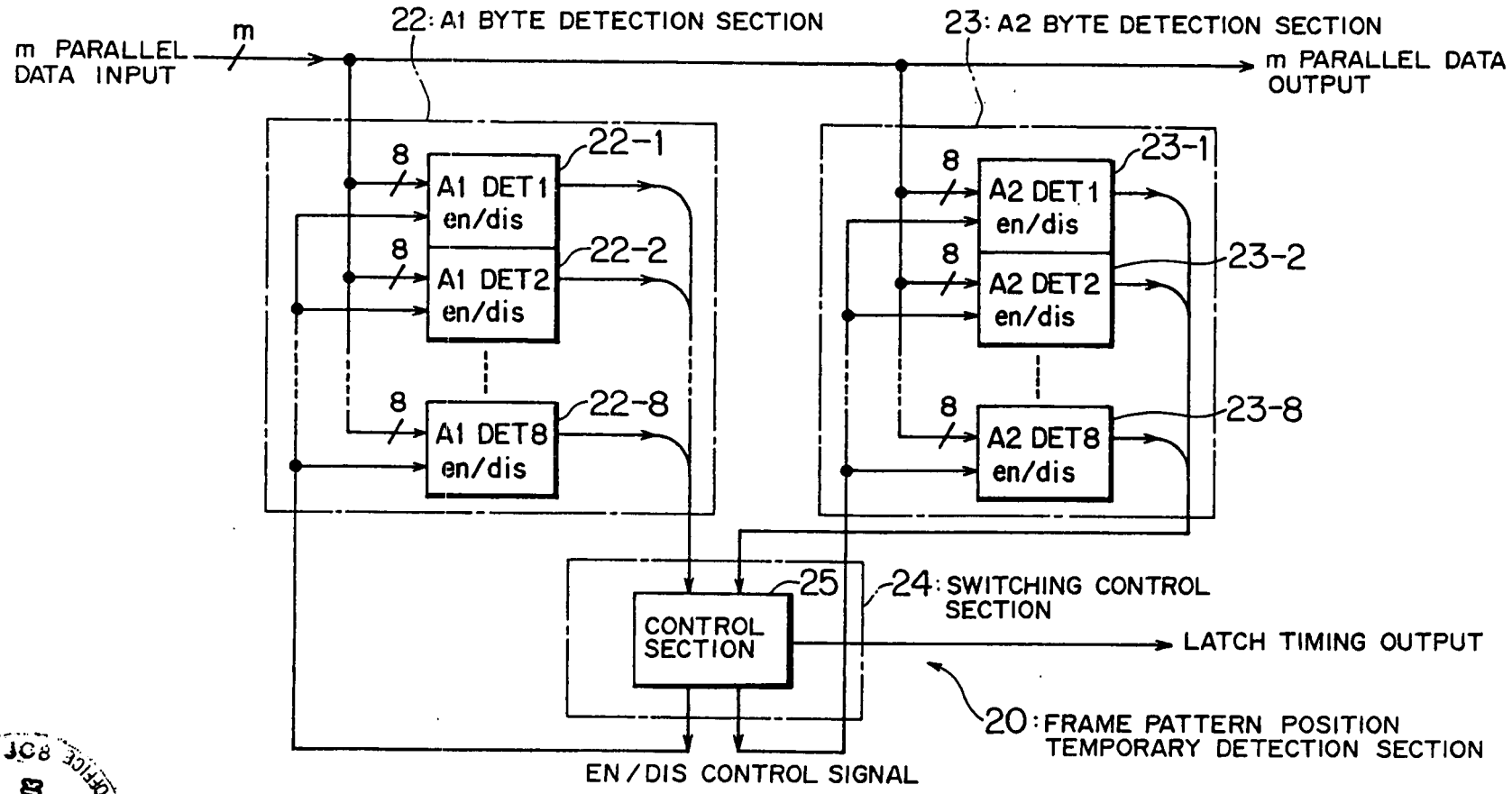


FIG. 10

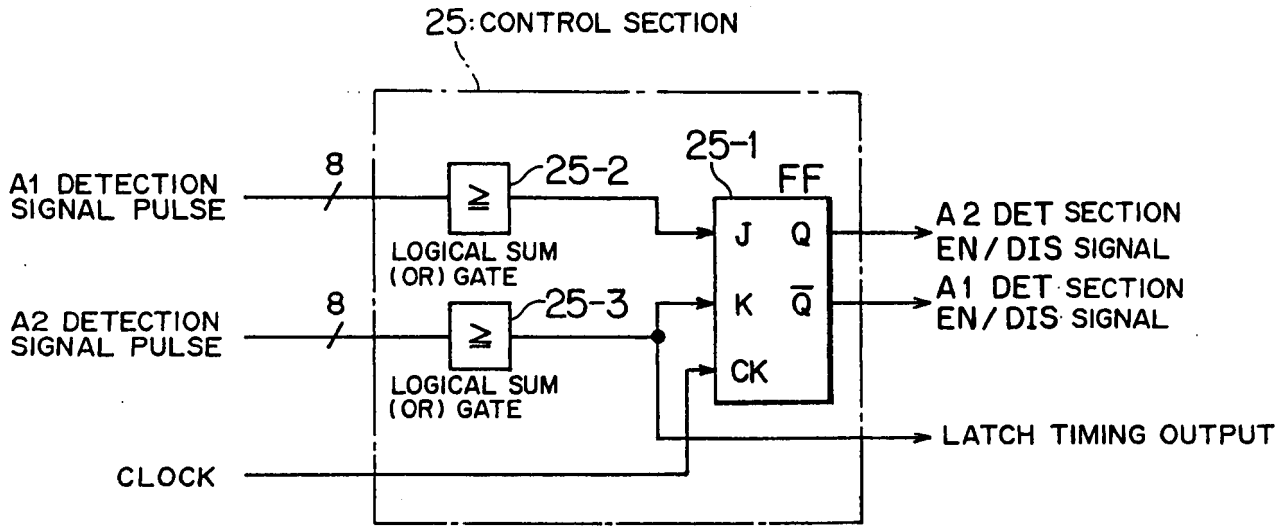


FIG. 11

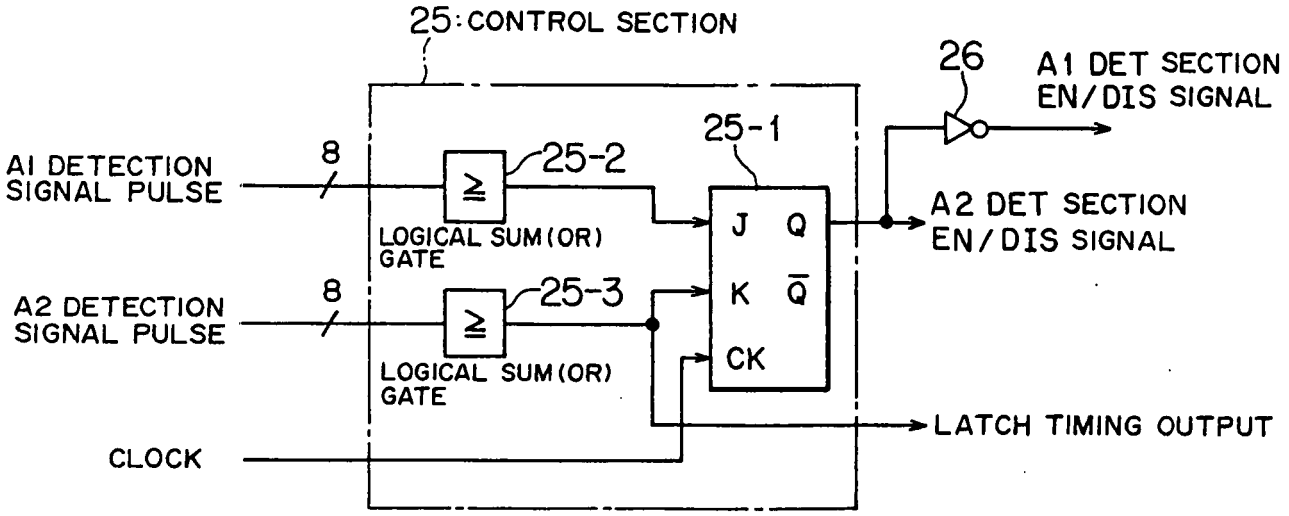


FIG. 12(a) m PARALLEL DATA

FIG. 12(b) A1 DET

FIG. 12(c) A2 DET

FIG. 12(d) EN/DIS SIGNAL

FIG. 12(e) LATCH TIMING OUTPUT

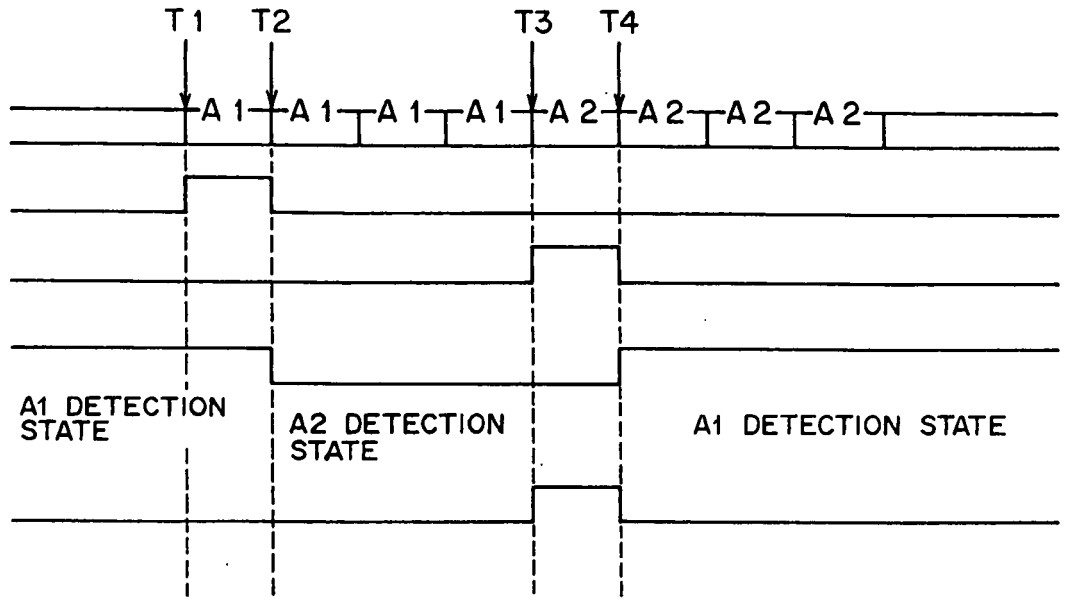


FIG. 13(a) CLOCK

FIG. 13(b) A1 DETECTION SIGNAL PULSE

FIG. 13(c) A2 DETECTION SIGNAL PULSE

FIG. 13(d) A2 DET SECTION EN/DIS SIGNAL

FIG. 13(e) LATCH TIMING OUTPUT

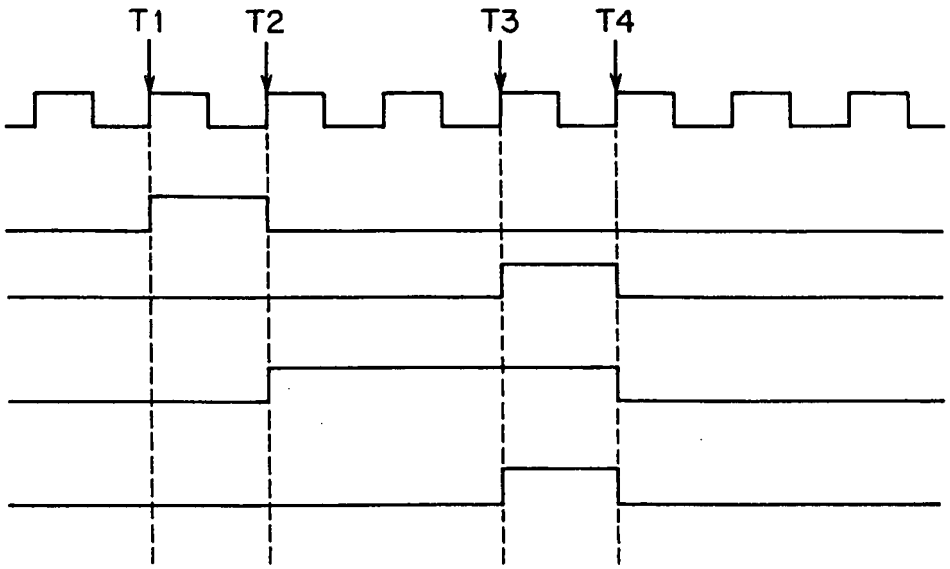


FIG. 14

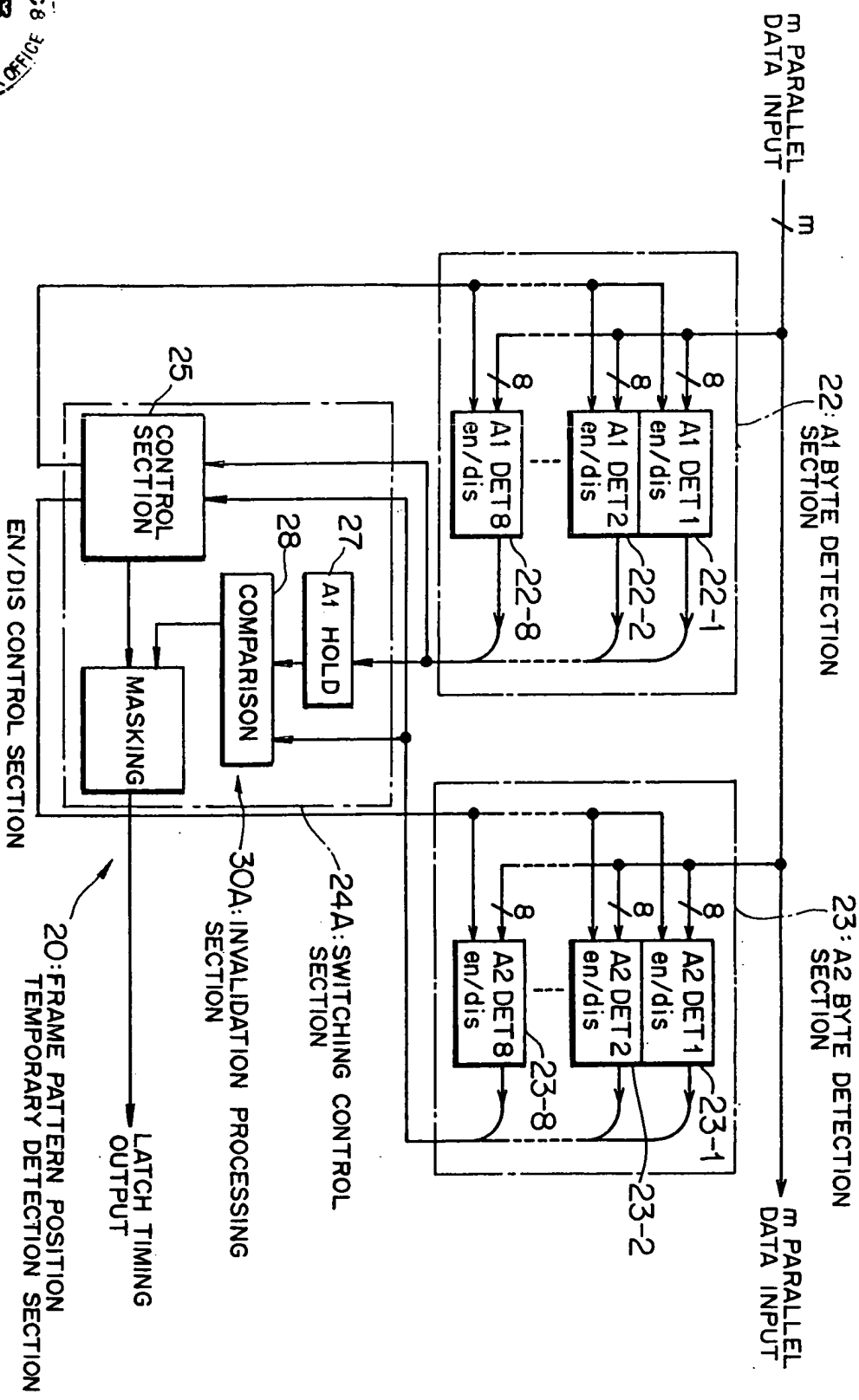
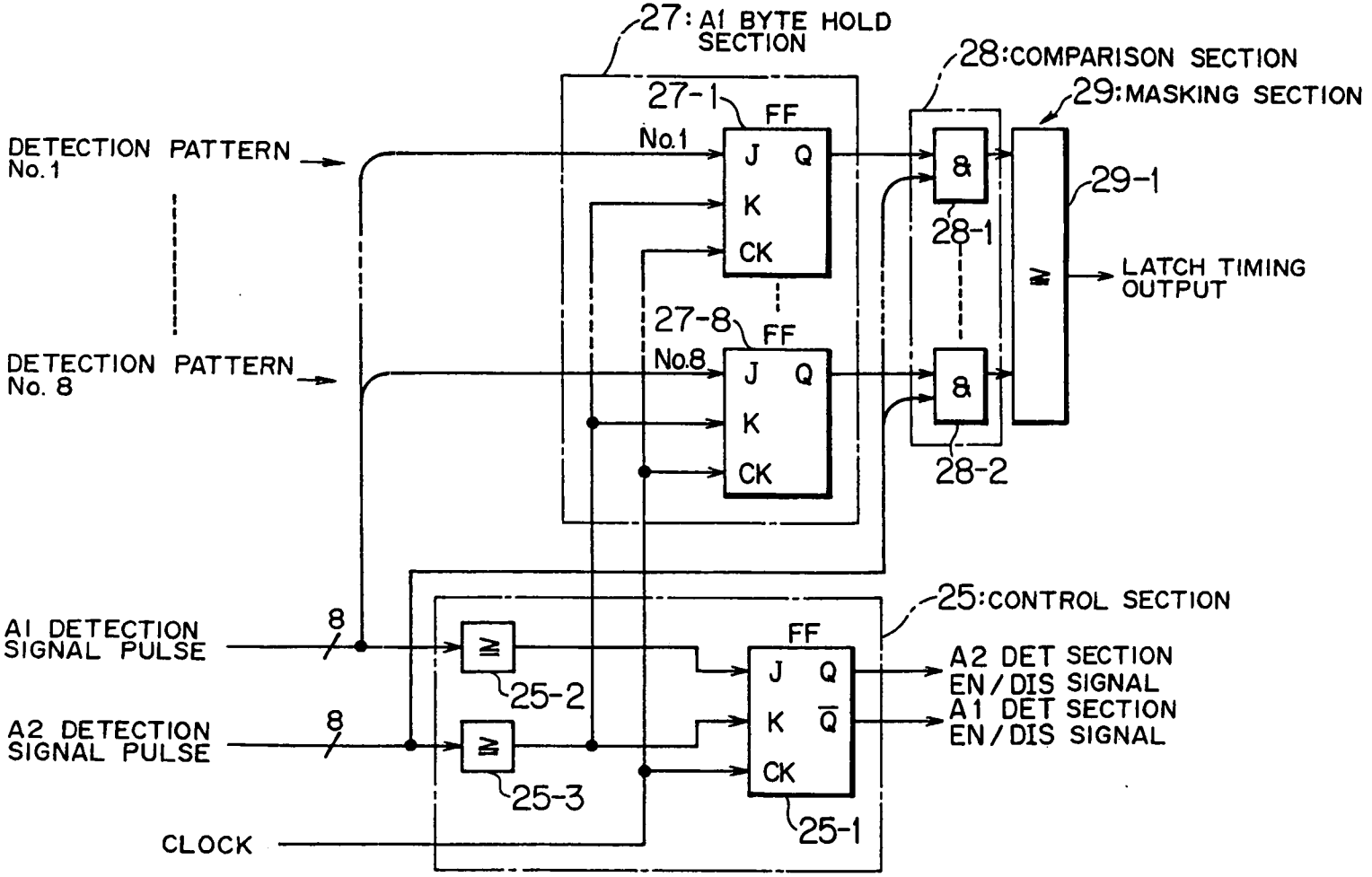


FIG. 15



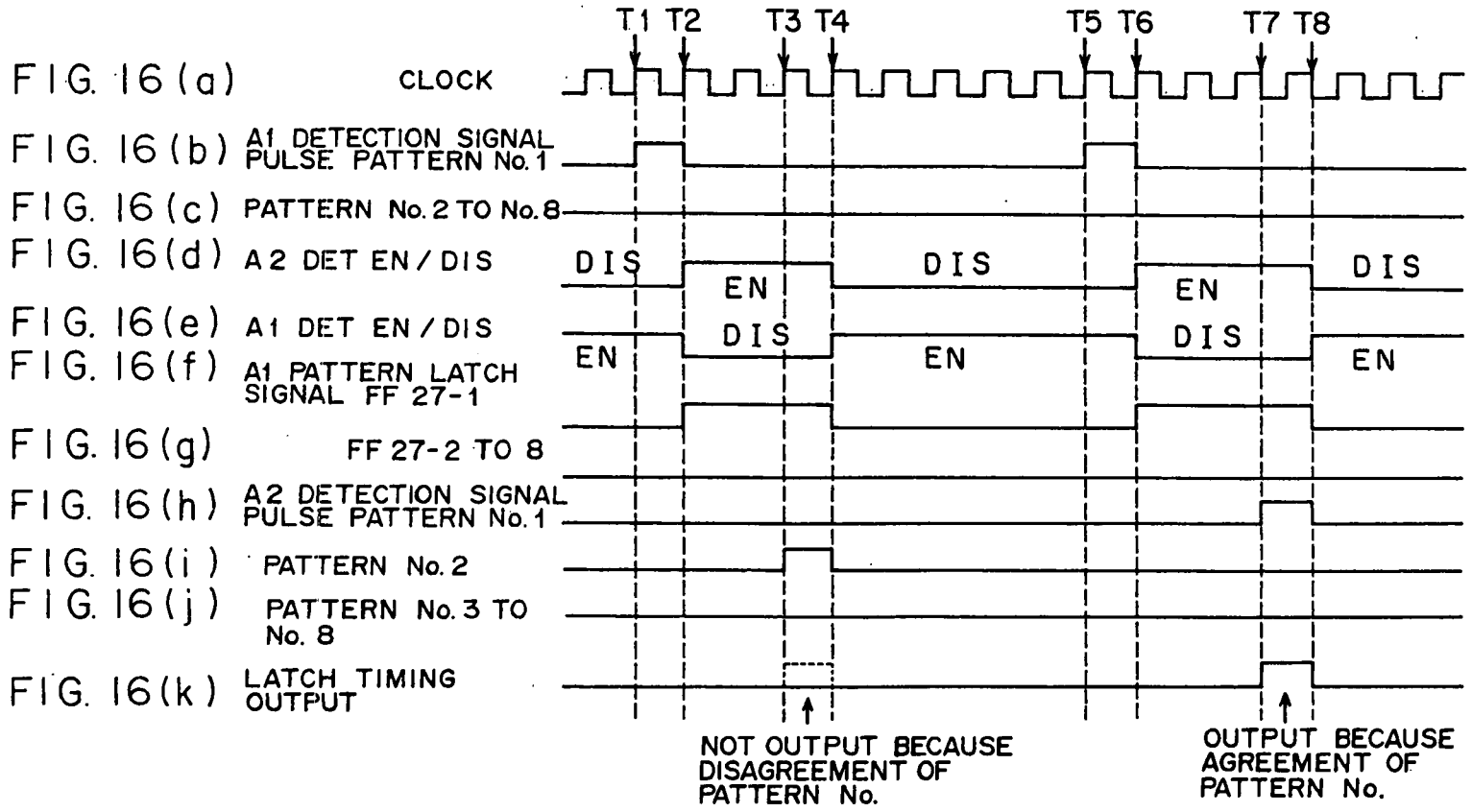
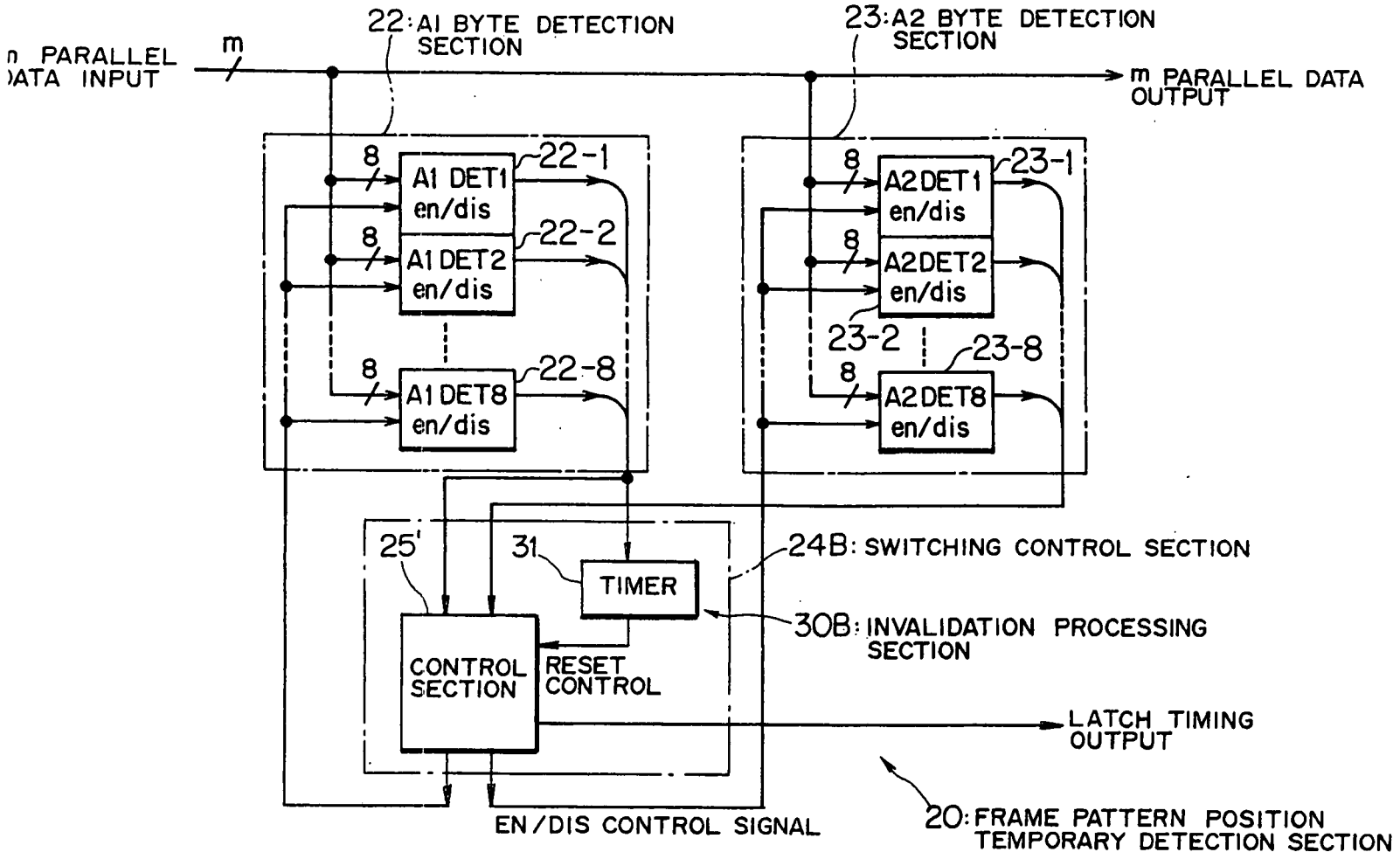


FIG. 17



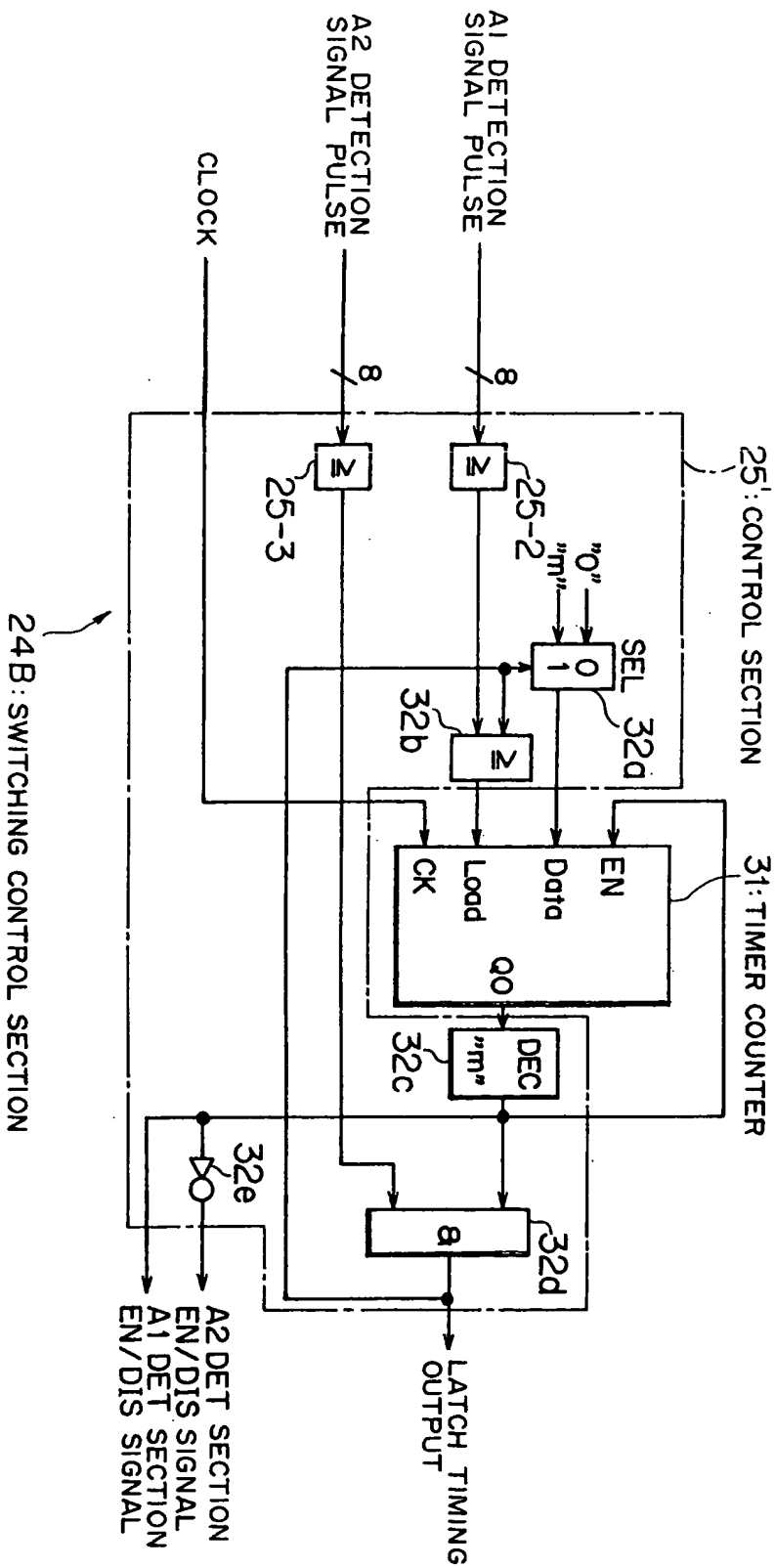


FIG. 18

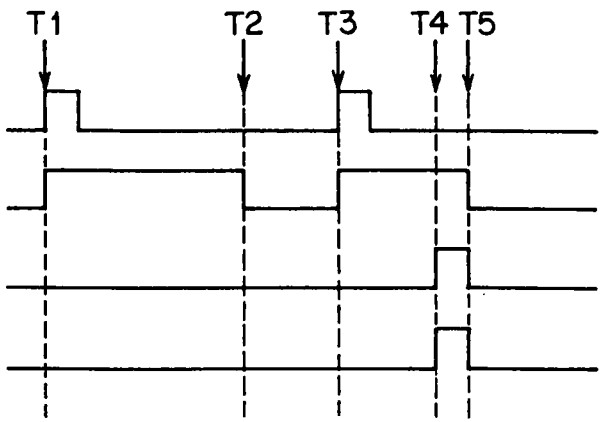


FIG. 19(a) LOAD INPUT

FIG. 19(b) Q OUTPUT

FIG. 19(c) A2 INPUT

FIG. 19(d) LATCH TIMING

FIG. 20(a) m PARALLEL DATA

FIG. 20(b) A1 DET

FIG. 20(c) A2 DET

FIG. 20(d) TIMER OUTPUT

FIG. 20(e) EN/DIS CONTROL SIGNAL

FIG. 20(f) LATCH TIMING OUTPUT

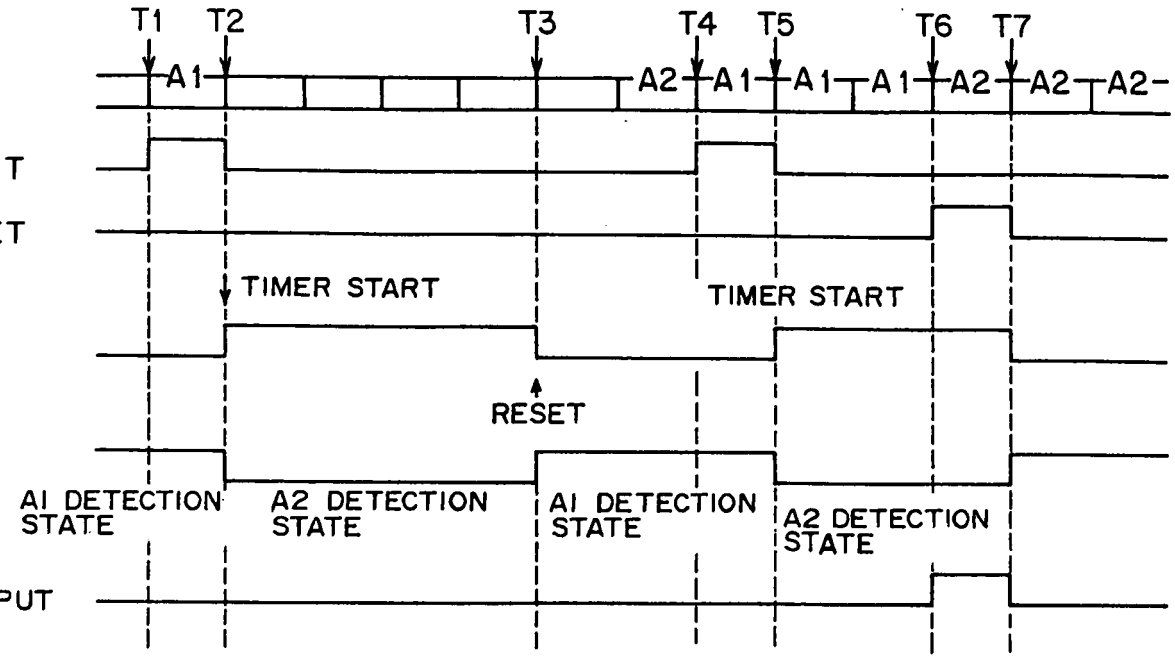


FIG. 21

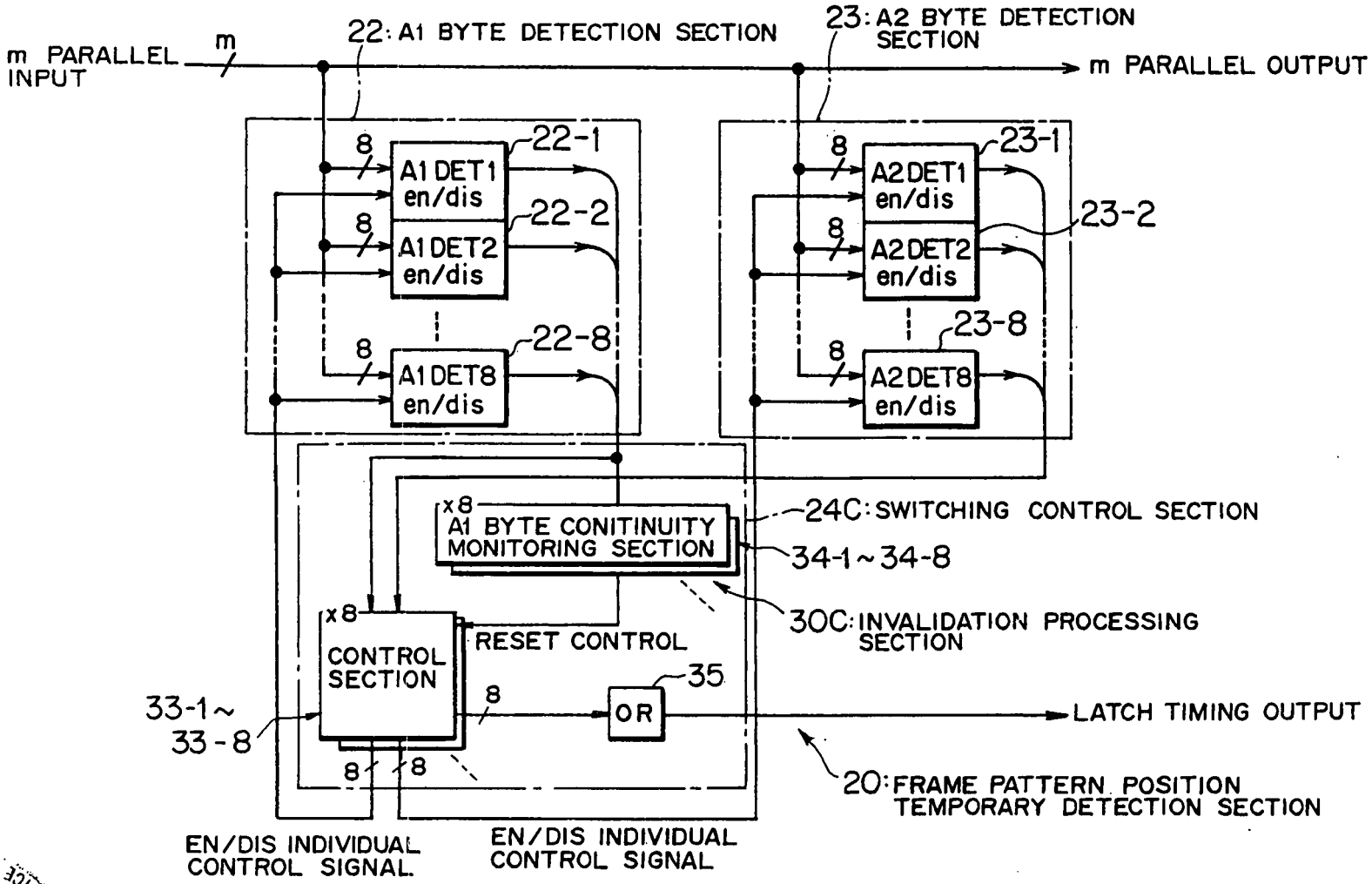


FIG. 22

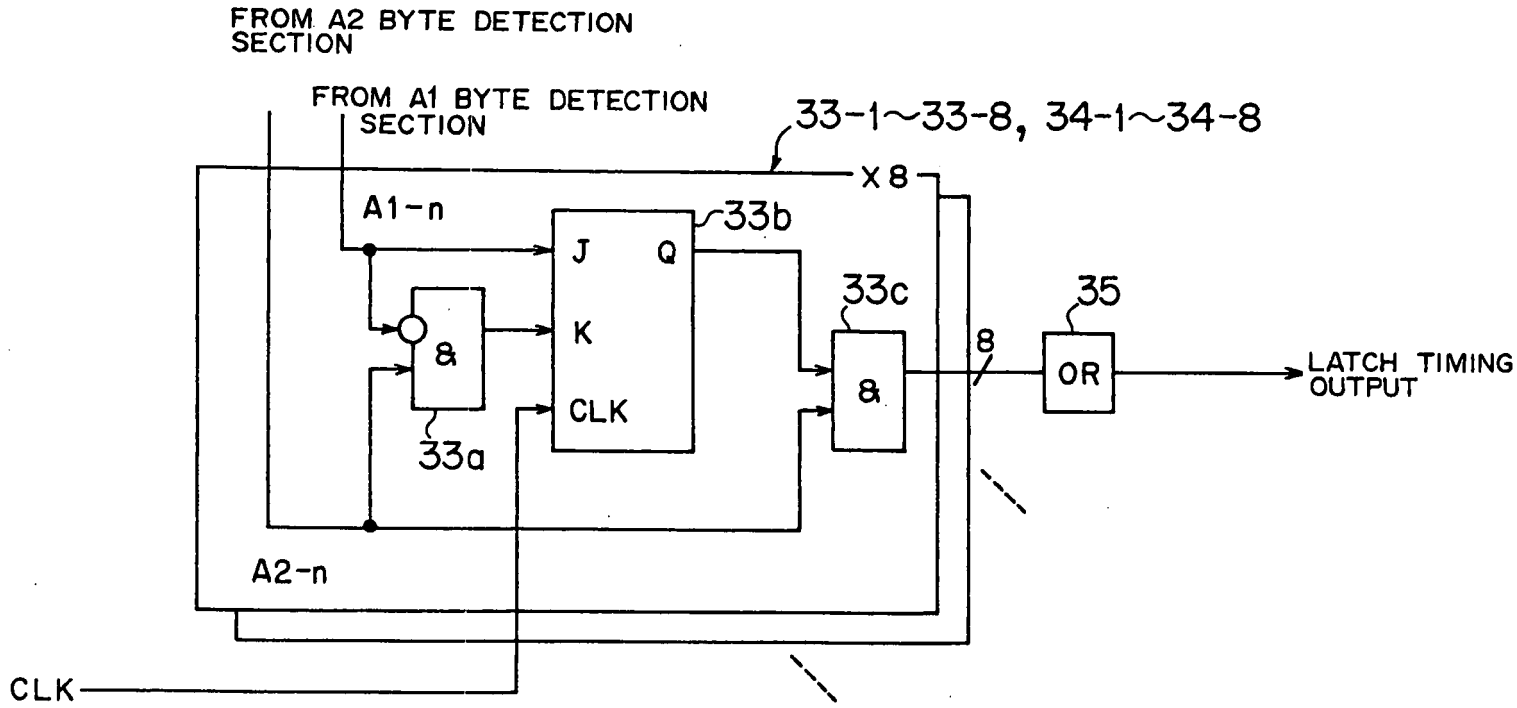


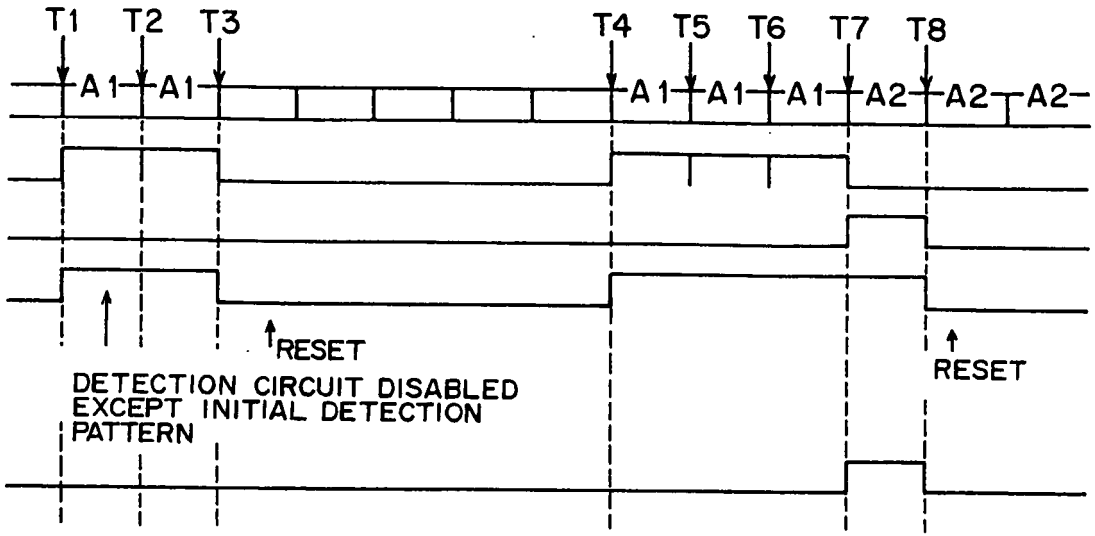
FIG. 23(a) m PARALLEL DATA

FIG. 23(b) A1 DET

FIG. 23(c) A2 DET

FIG. 23(d) EN/DIS CONTROL

FIG. 23(e) LATCH TIMING OUTPUT



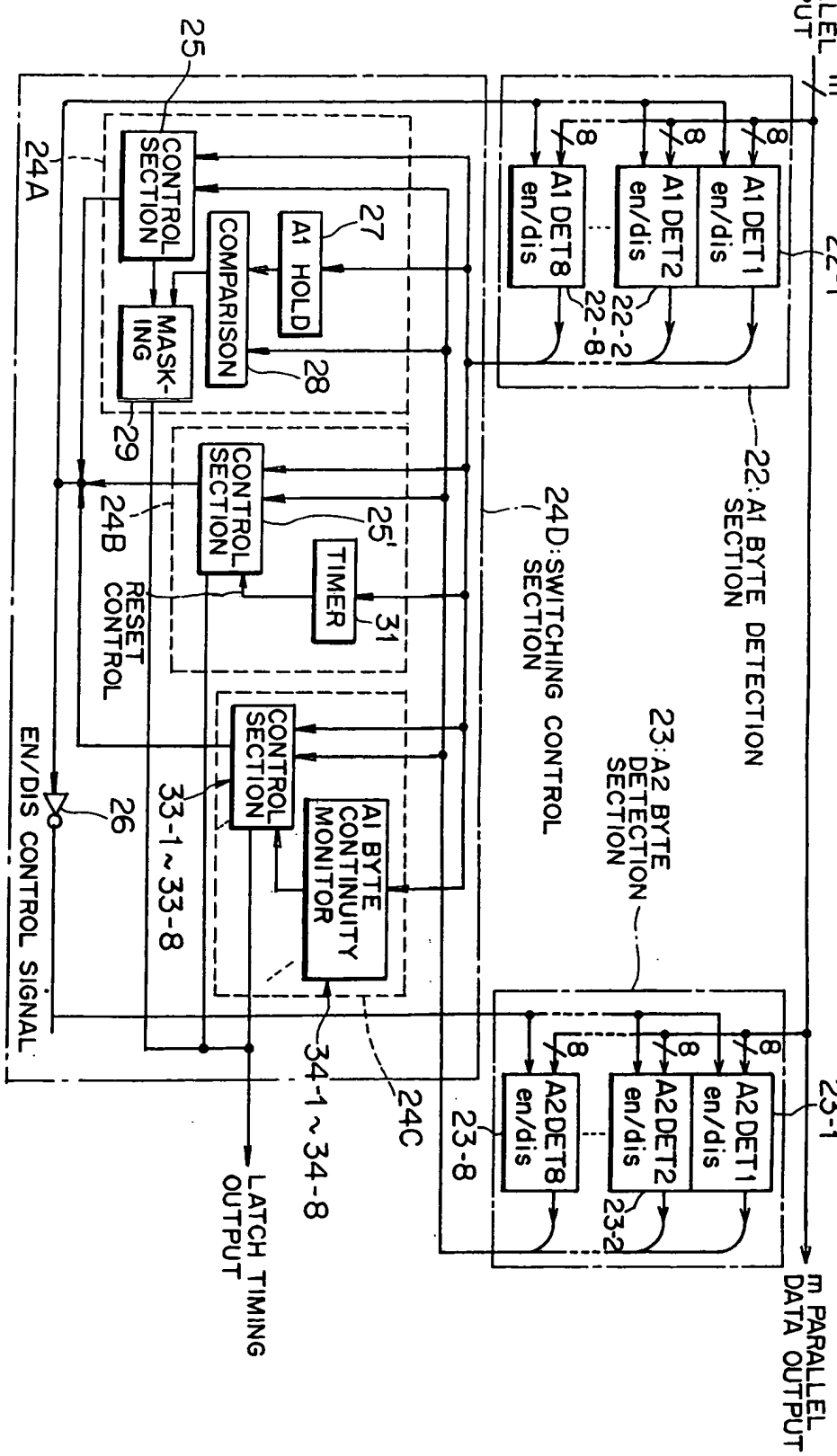
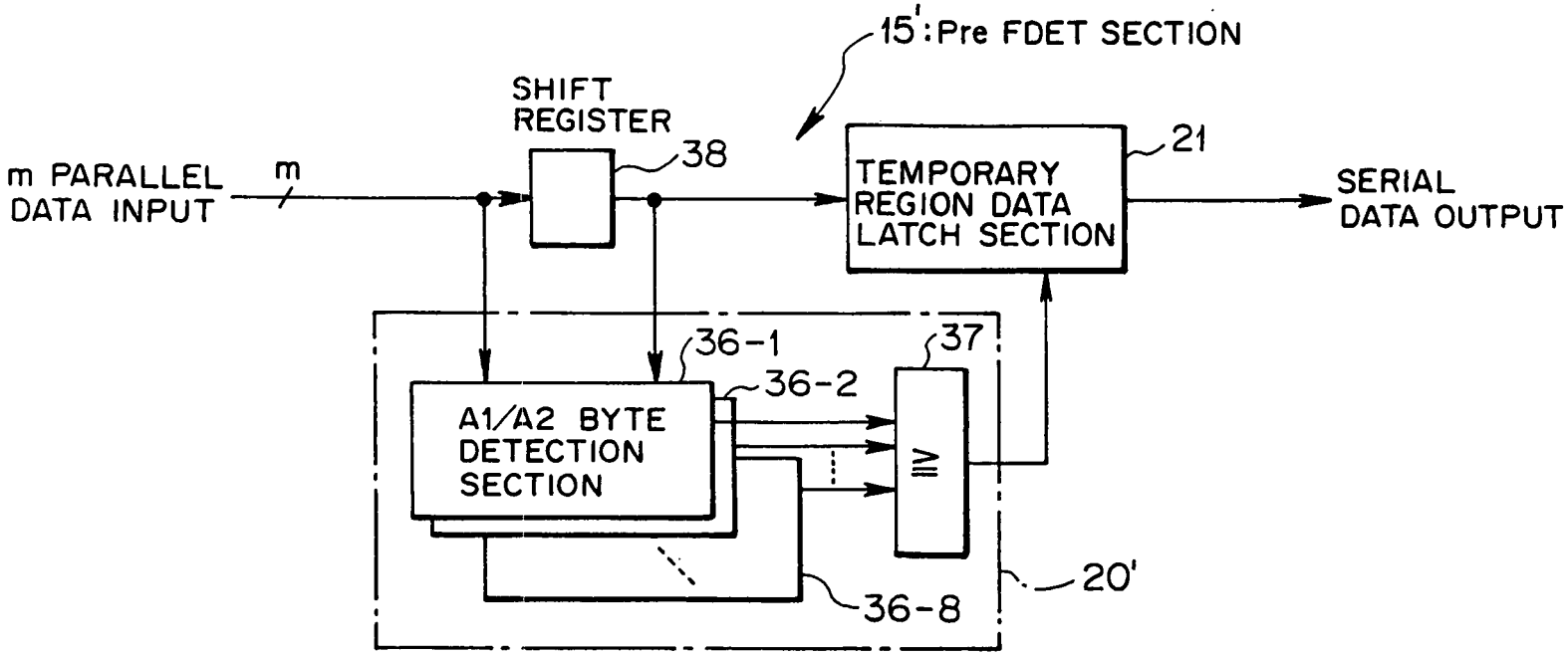


FIG. 24

FIG.25



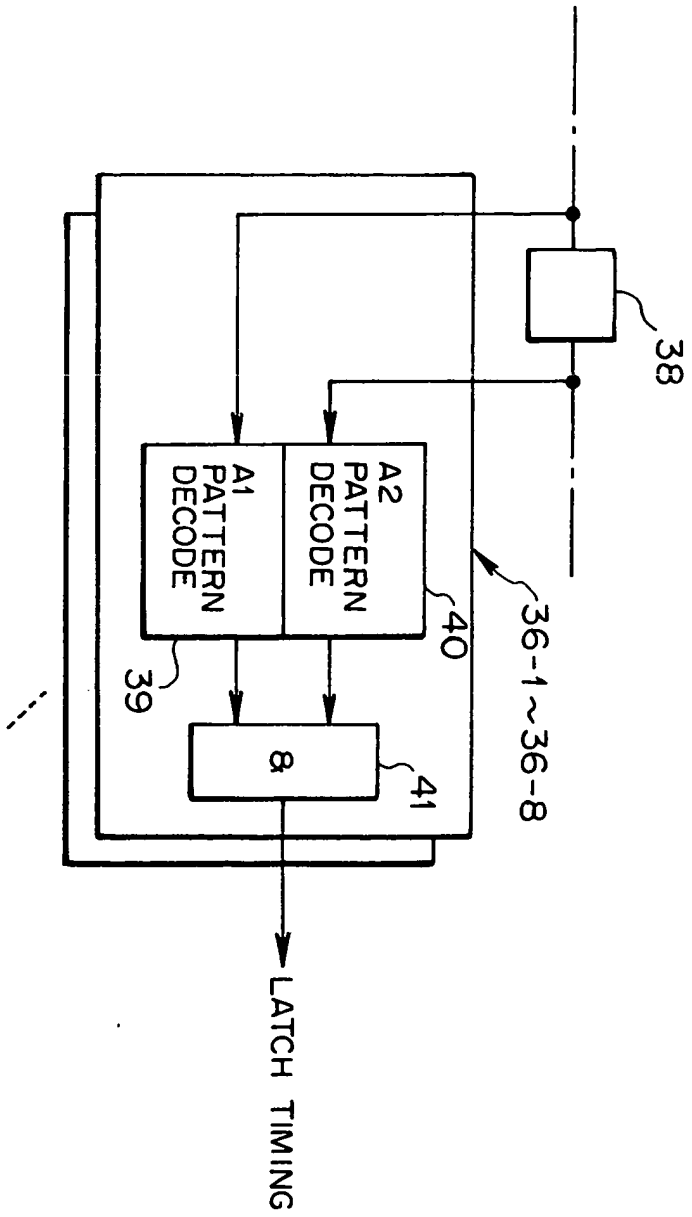


FIG.26

FIG. 27(a)

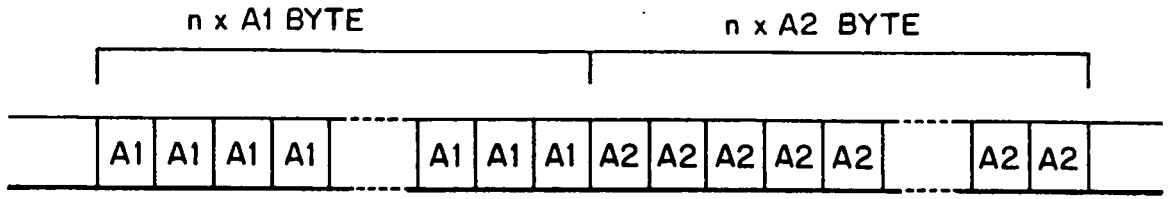


FIG. 27(b)

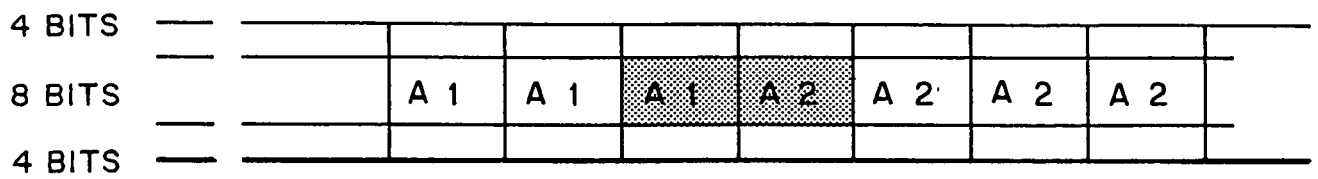
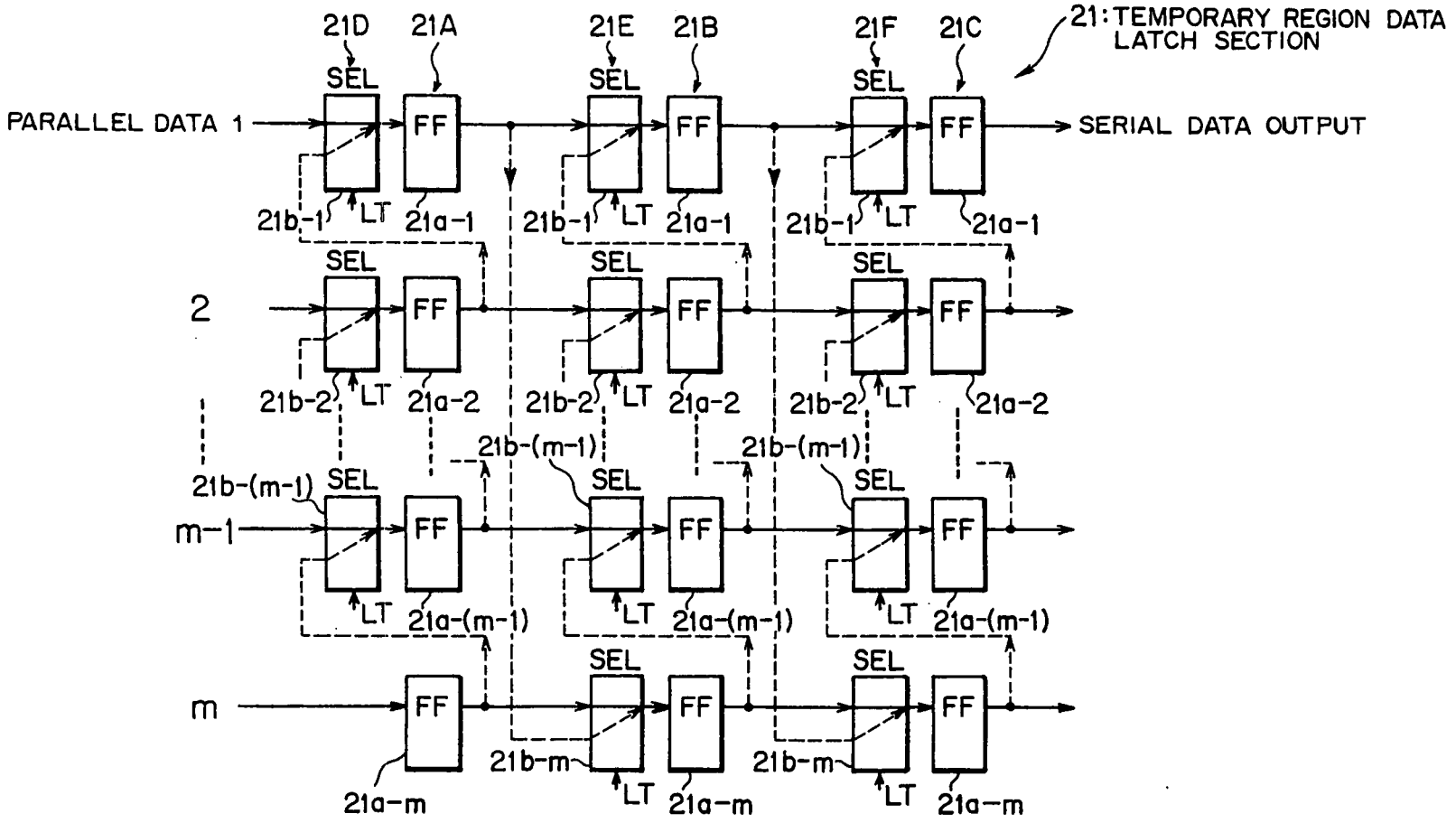
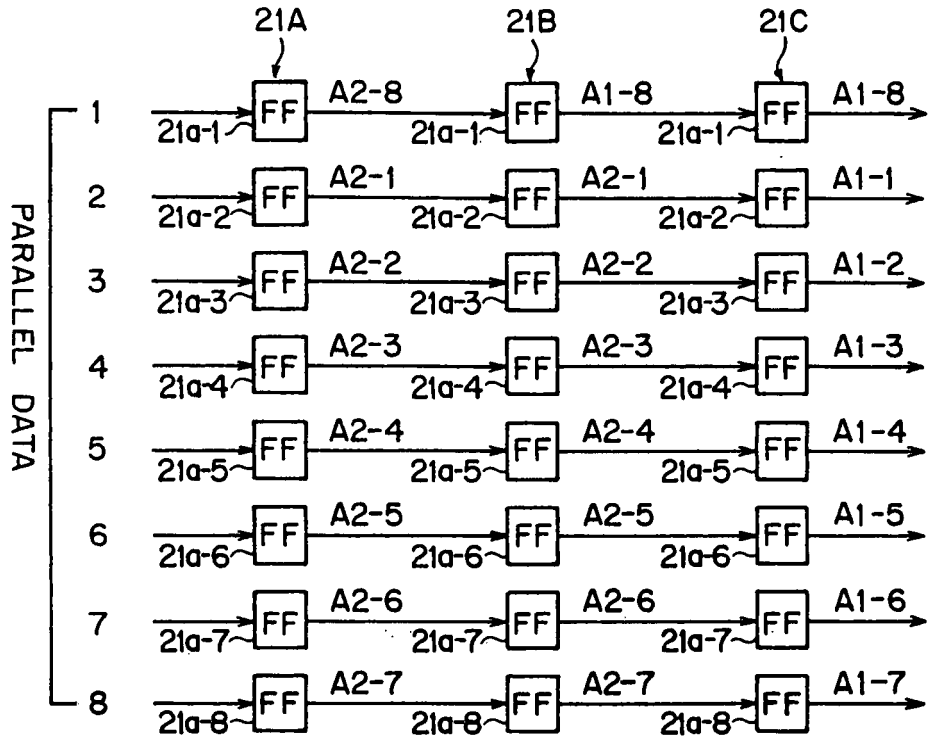


FIG. 28



LT: LATCH TIMING SIGNAL

FIG. 29



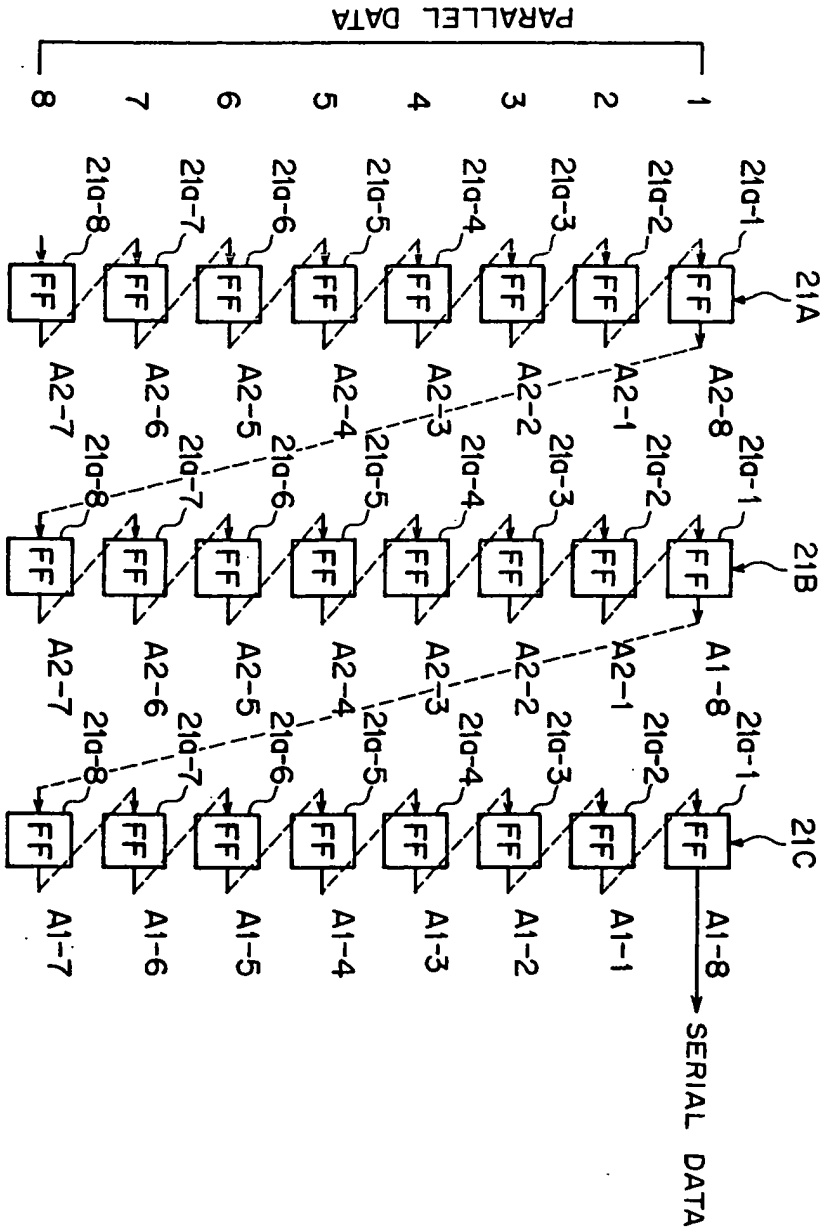


FIG. 30

FIG.31

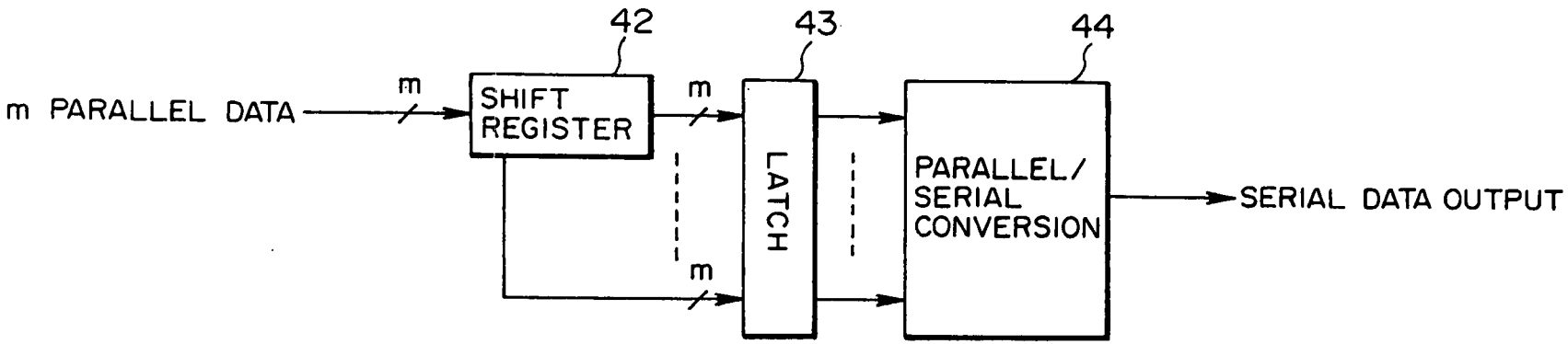


FIG.32

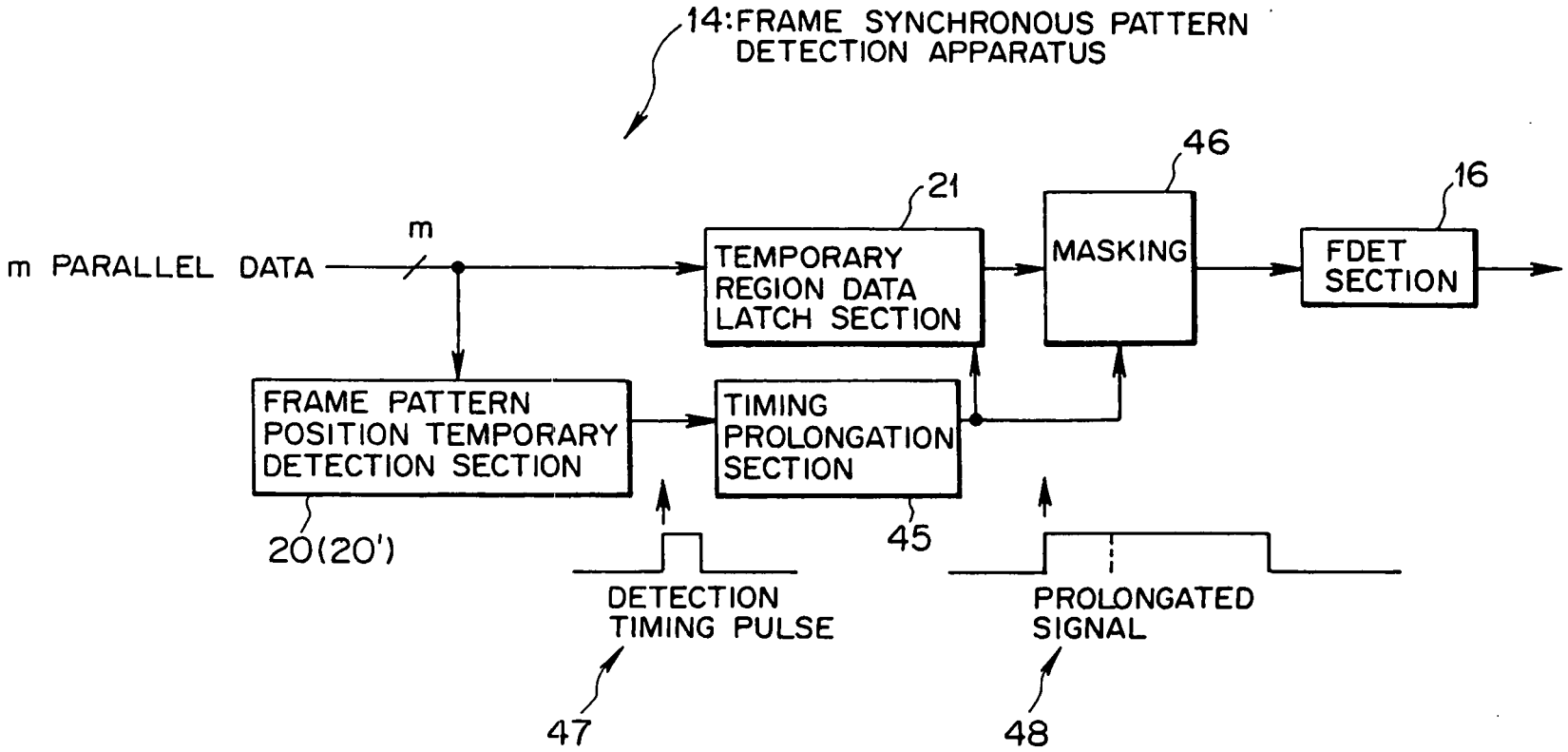


FIG. 33

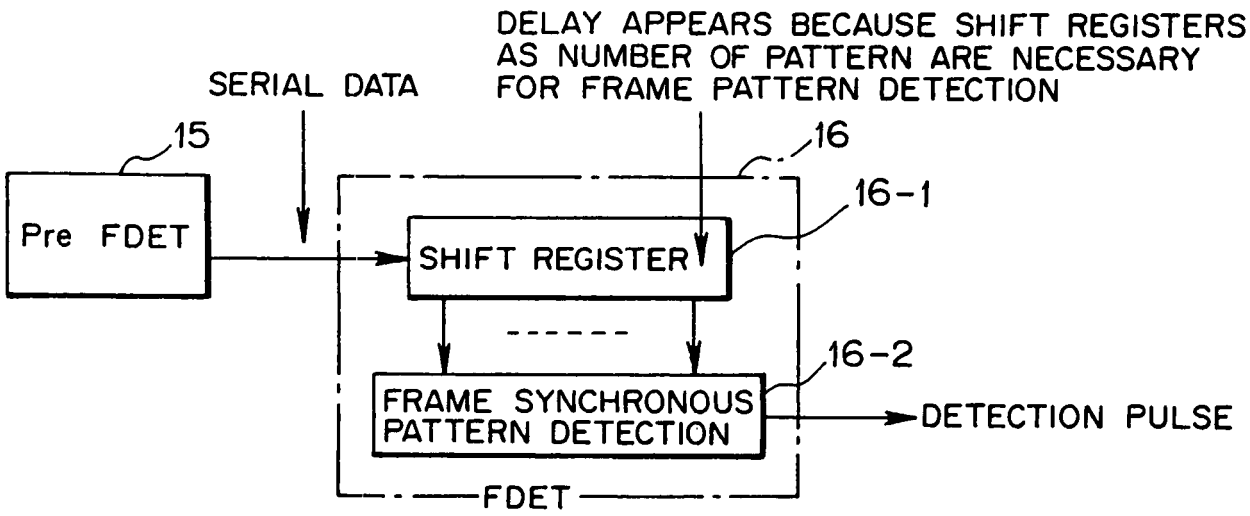


FIG. 34

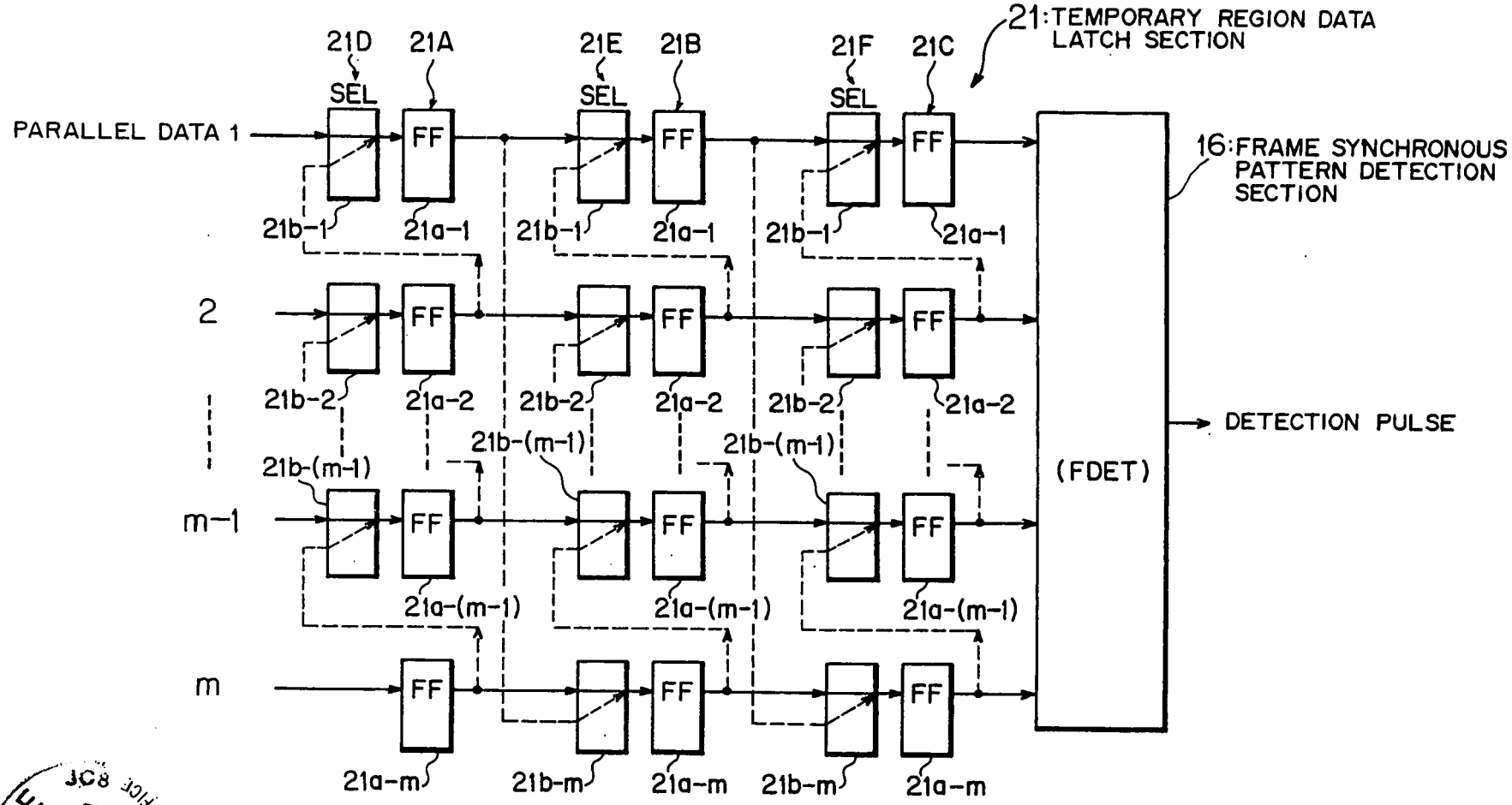


FIG. 35

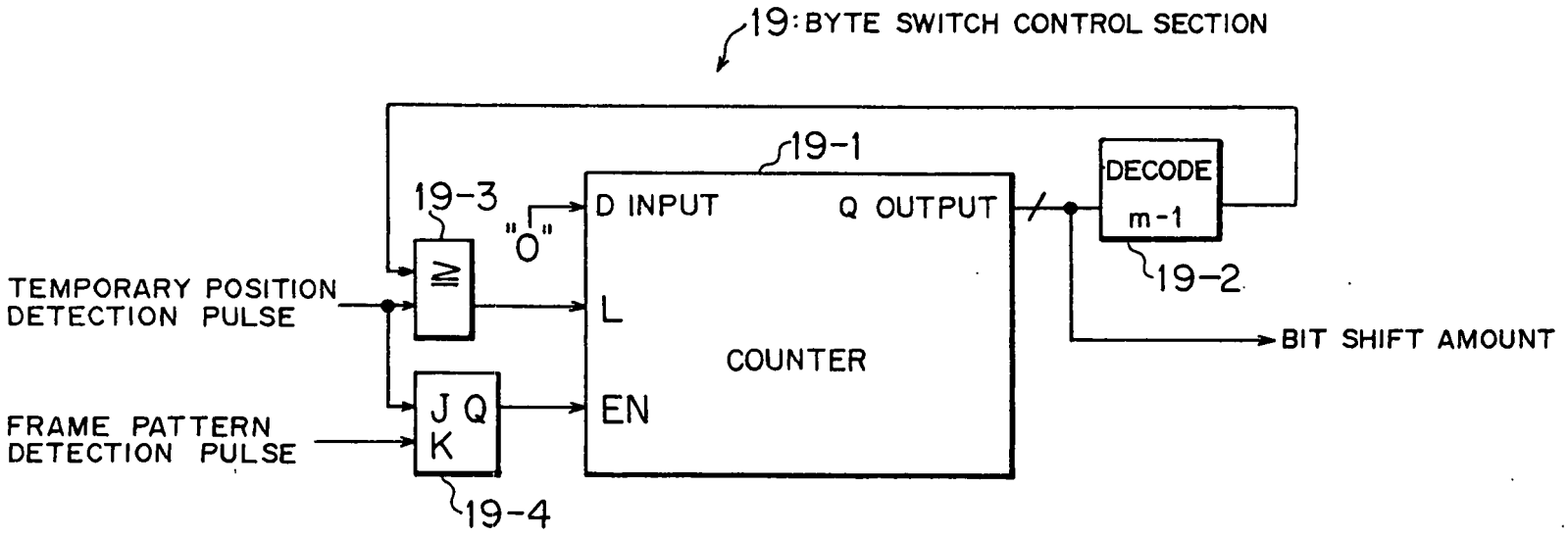


FIG. 36(a)

FIG. 36(b)

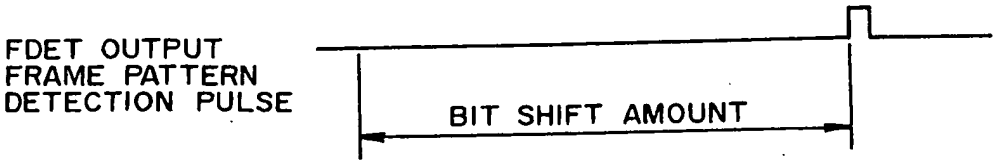


FIG. 37

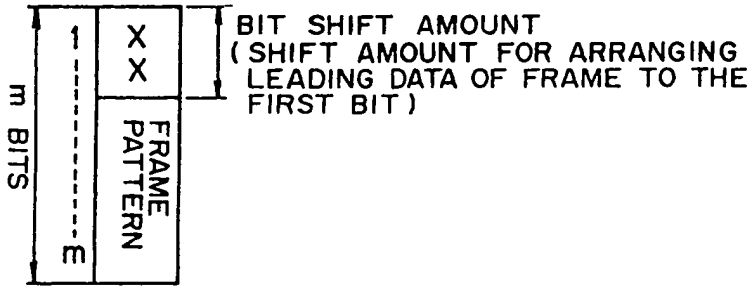


FIG. 38

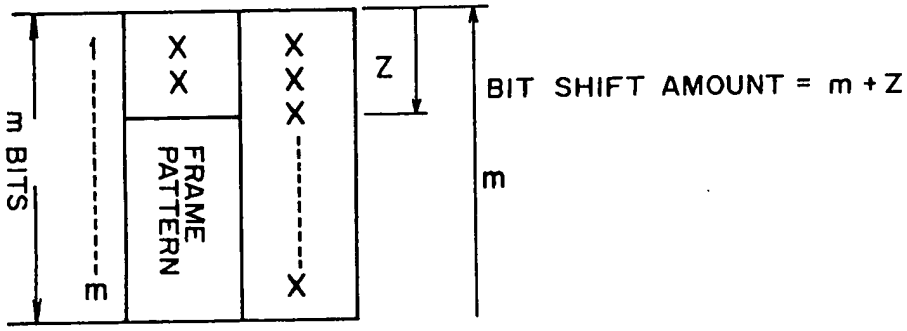


FIG. 39(a) TEMPORARY POSITION DETECTION PULSE

FIG. 39(b) FRAME PATTERN DETECTION PULSE

FIG. 39(c) COUNTER EN (ENABLE)

FIG. 39(d) COUNTER L (LOAD)

FIG. 39(e) COUNTER L VALUE

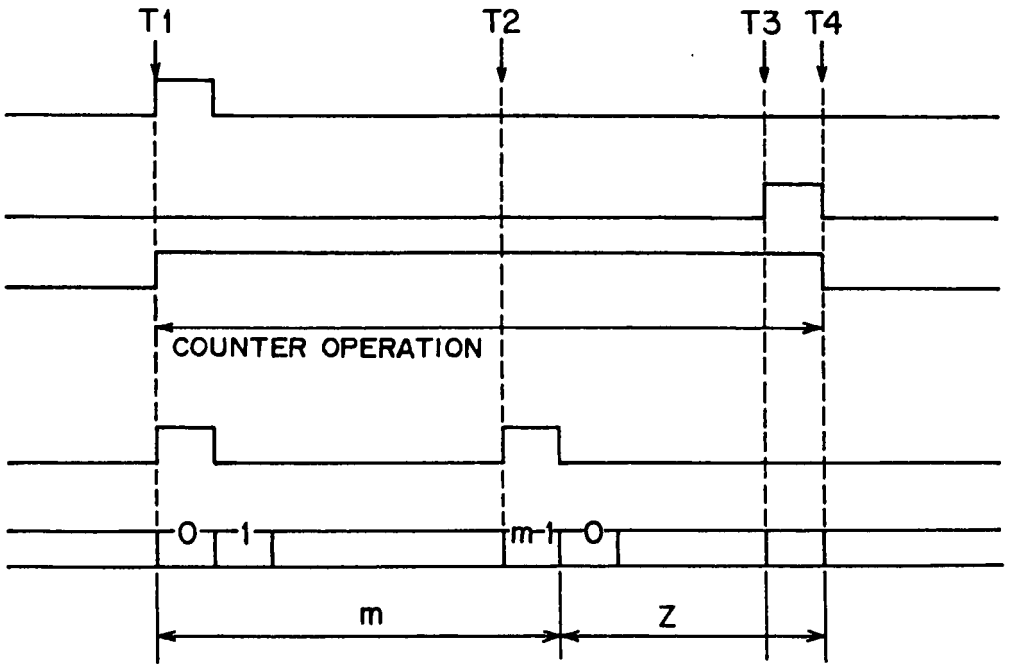


FIG. 40
PRIOR ART

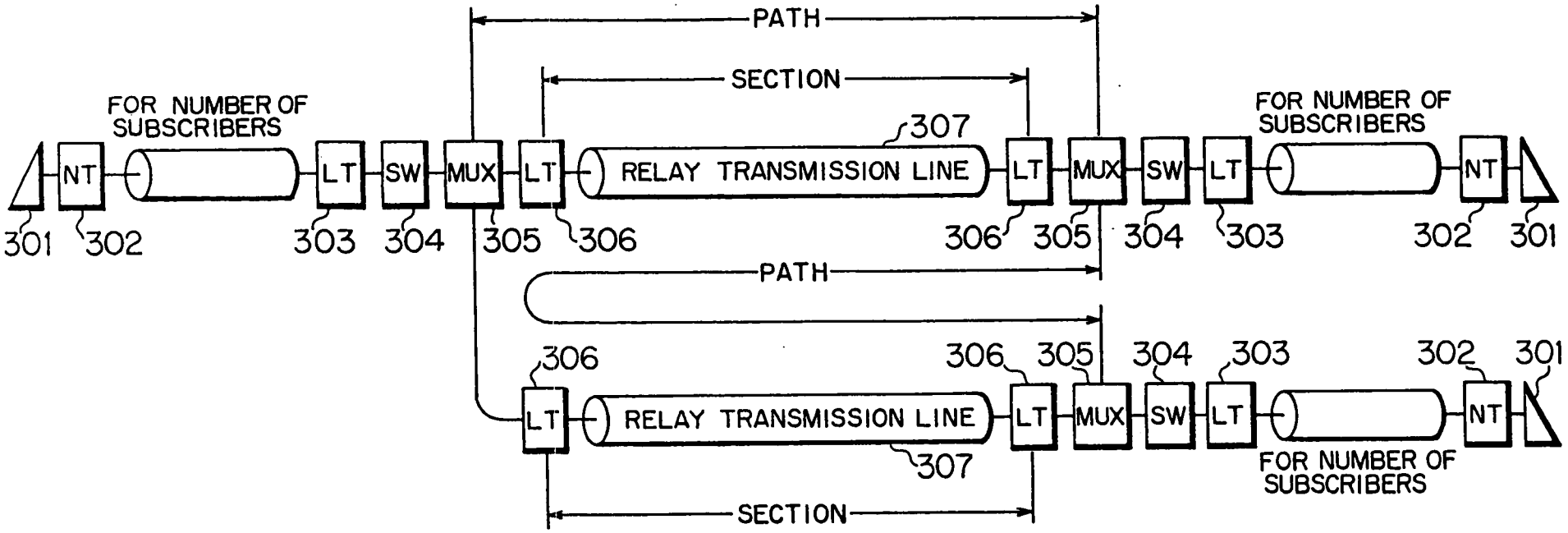


FIG. 41
PRIOR ART

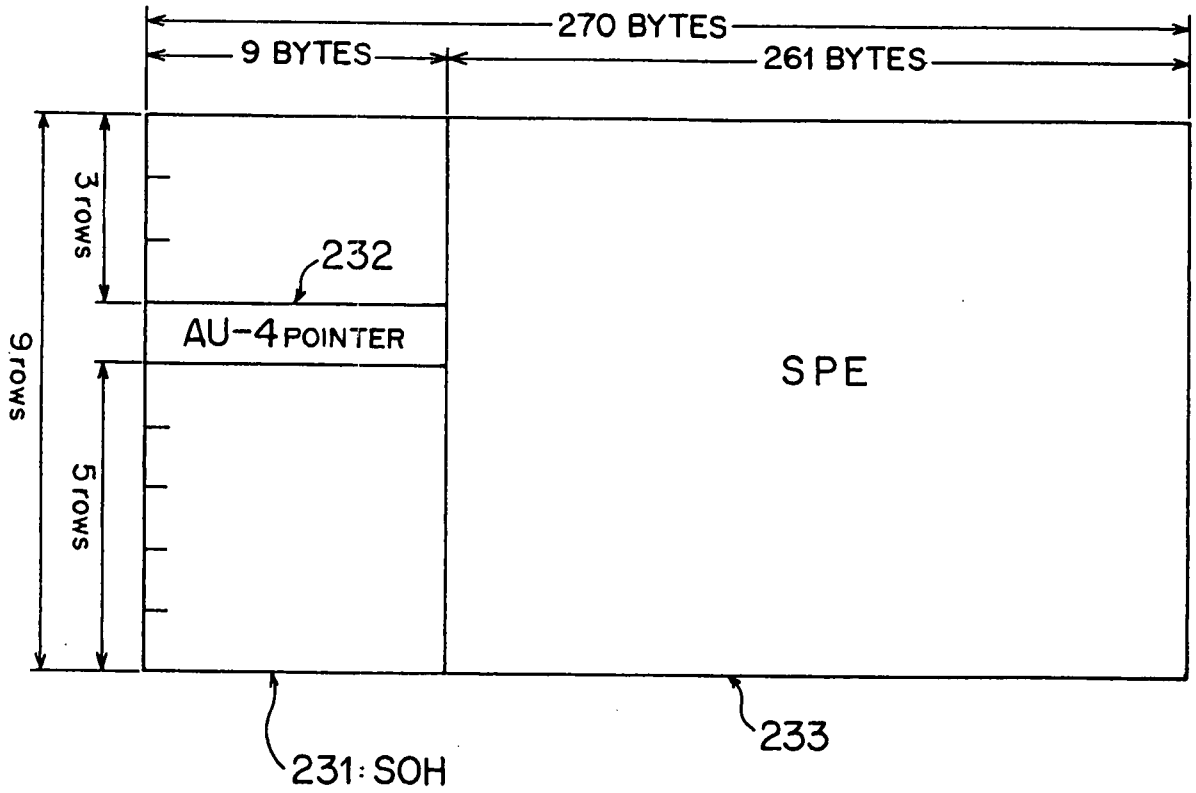


FIG. 42
PRIOR ART

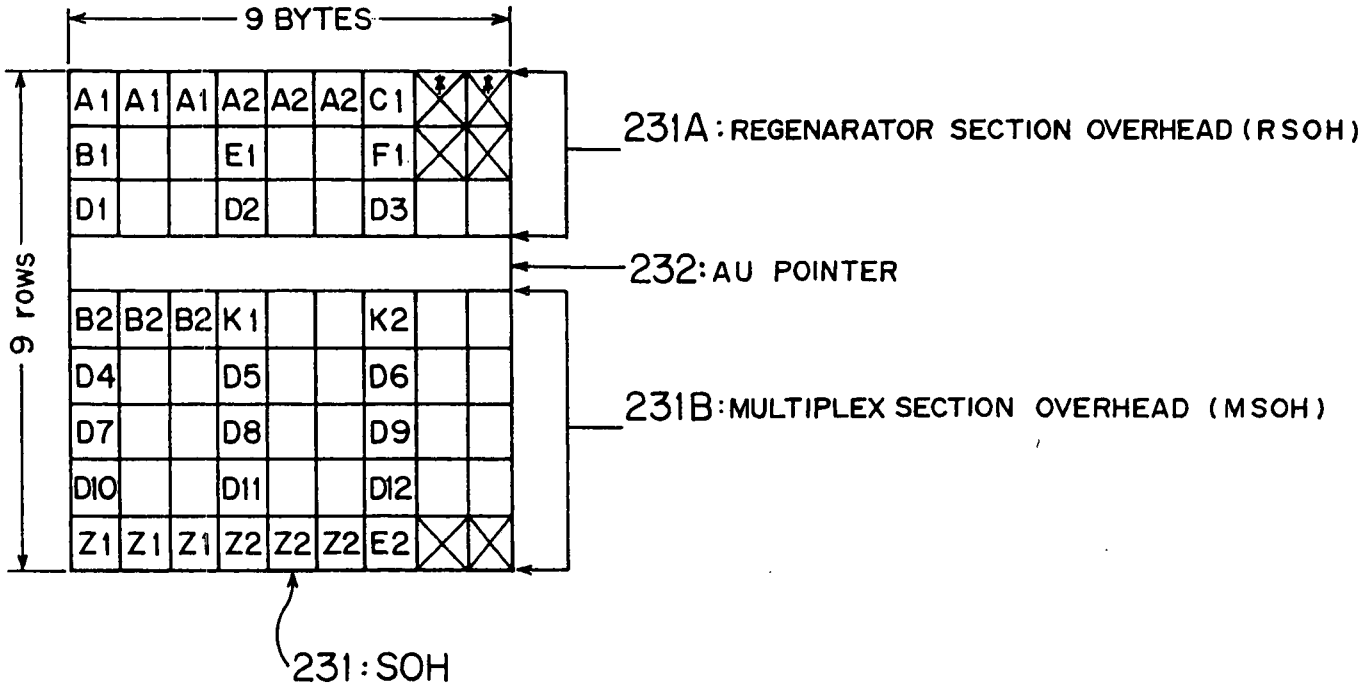


FIG. 43
PRIOR ART

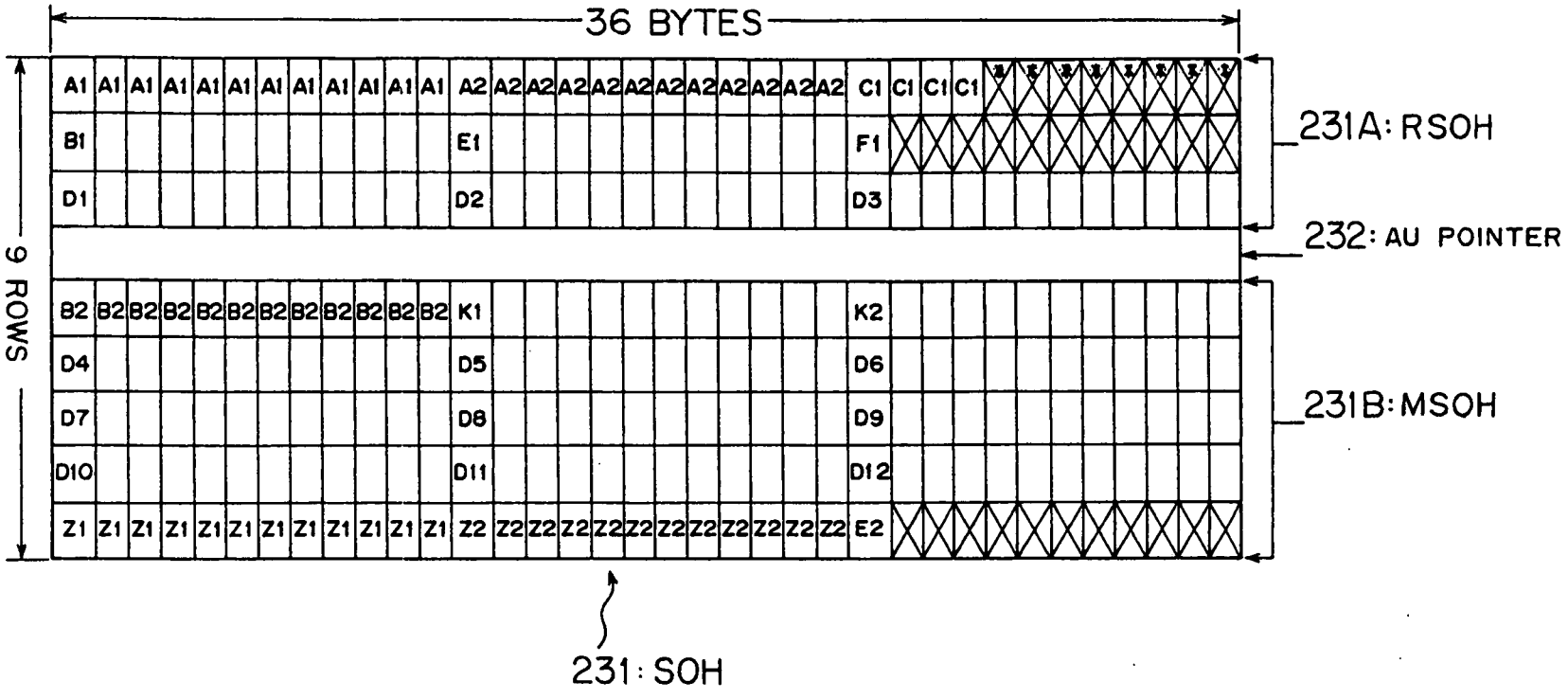


FIG.44
RELATED ART

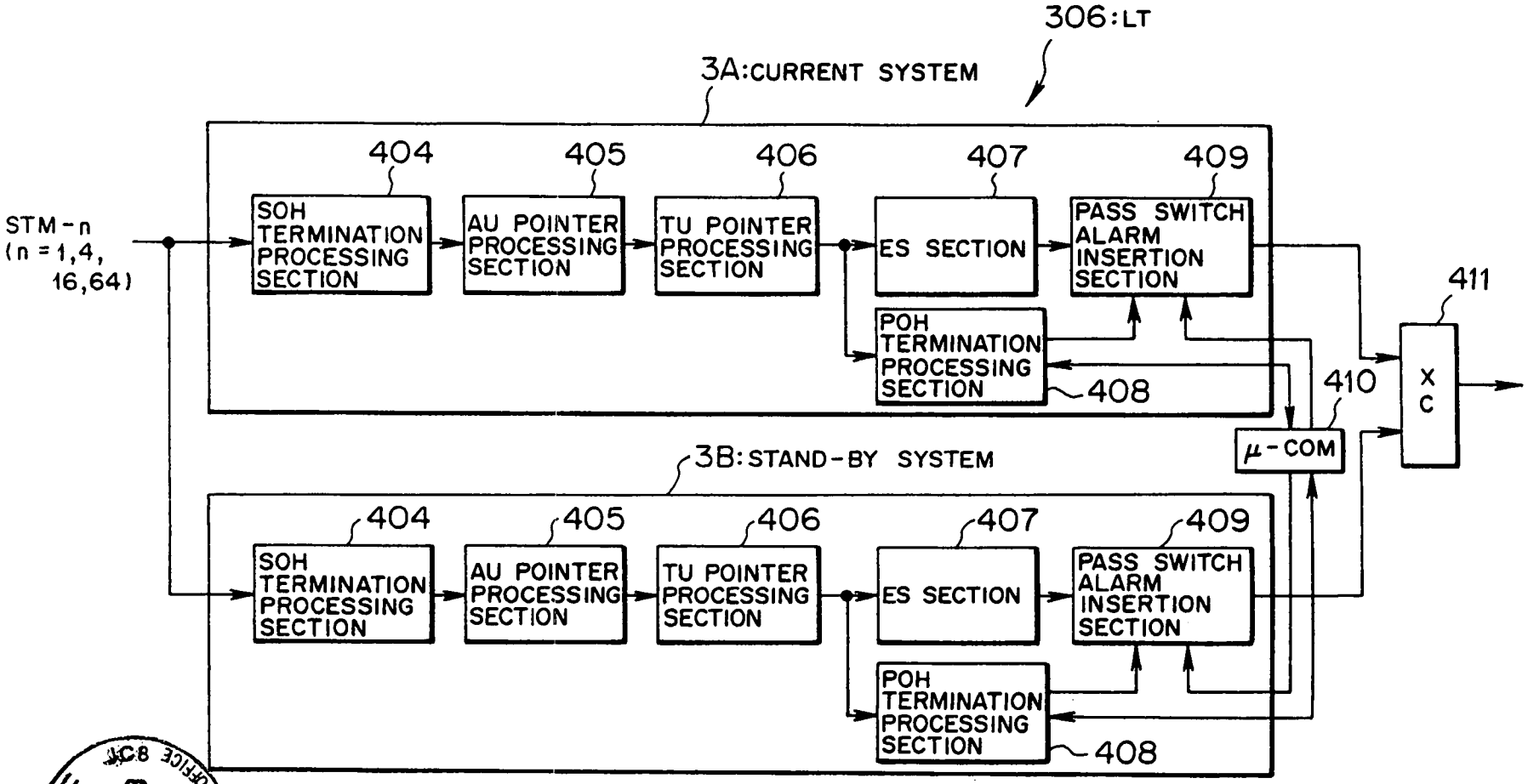


FIG. 45
RELATED ART

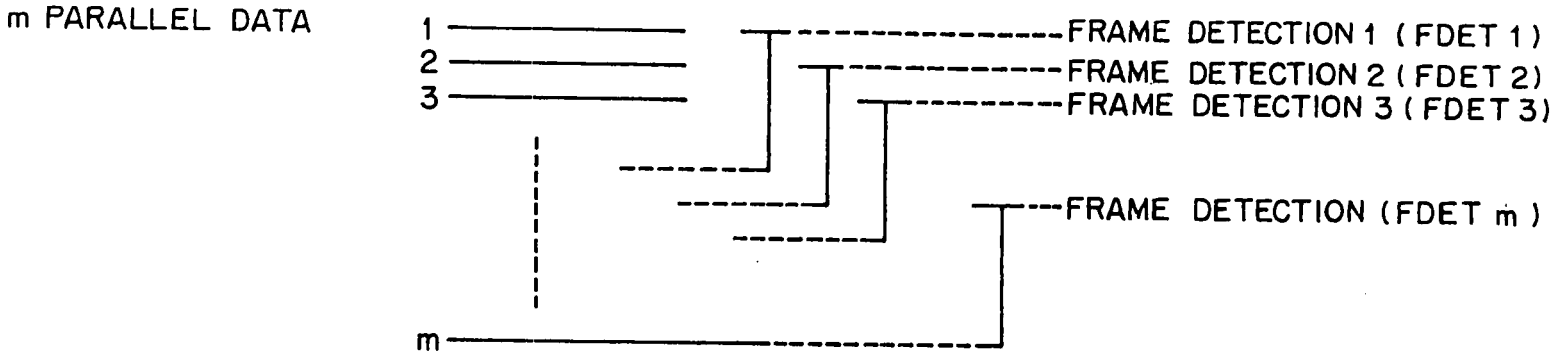


FIG.46
RELATED ART

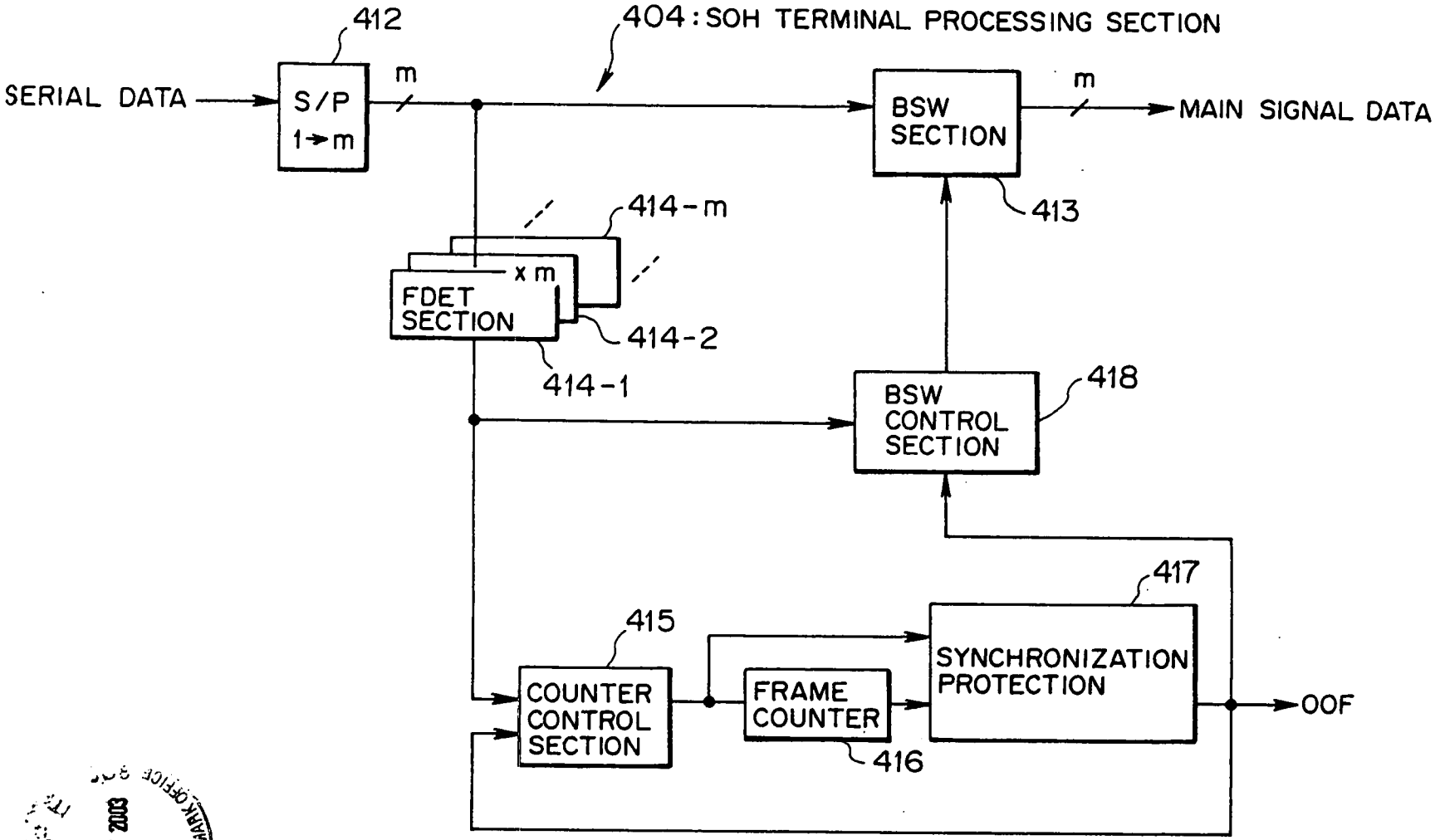


FIG.47
RELATED ART

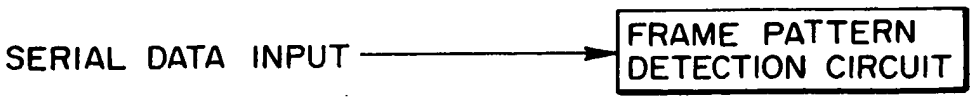


FIG.48
RELATED ART